Addressing Today's Challenges of High-Speed Interconnect Test

Submitted by Keysight Technologies

Achieving high volume production test or R&D prototype test of high-speed interconnects, such as cables, backplanes, PCBs and connectors requires a fast, automated physical layer test system. Engineers need a test system that can keep up with the latest technologies and use leading edge test equipment and software. Fast paced manufacturing test requires a system with user definable flexibility, and a user-friendly interface to simplify test configurations and execution for signal integrity engineers. Breakthrough technologies have increased computer and network system's data rates resulting in interconnection design updates adding to the complexity of physical layer test.

This article describes the challenges and needs for physical layer test today and in the near future.

Signal integrity engineers are discovering new test challenges as the development of next generation computer and communication system exceed data rates of multiple gigabits per second. Processors and SERDES chip sets, within these systems, are expected to operate beyond Giga hertz clock frequencies. Demand for higher data rates resulted in several physical layer design changes including signal routing for higher data rates and higher bandwidth per pin in high-speed serial bus designs by transitioning from parallel bus structures to serial bus structures. Design engineers are also implementing differential circuits instead of single-ended circuits in order to maintain channel signal integrity, minimize effect of cross talk, and enable maximum data rate throughput.

In addition to testing issues related to new serial interconnects, there are also new issues with switches, router, server blades and storage area networking equipment due to the higher data rates. The differential transmission lines create design and test difficulties due to their susceptibility to microwave effects with high speed data. New circuit designs and high-speed digital system performance has become a limiting factor in physical-layer structure which includes increased clock speeds, bus speed and link speed, making physical layer characterization more important than ever.

Digital design engineers require an understanding of the fundamental properties of signal propagation through measurement and post measurement analysis, as well as new design and validation tools, for today's telecommunication and computer systems. Both time domain and frequency domain measurements are important during physical layer test and analysis. Time domain analysis helps with characterization of physical-layer structures and requires step and impulse responses in reflection and transmission (TDR and TDT) for a full time-domain view. Frequency domain analysis is needed to fully characterize physical-layer structures such as s-parameters, which describe the analog behavior of the digital structures. The behaviors include

reflections from discontinuities, frequency dependent losses, crosstalk, and EMI performance. Signal integrity engineers need new capabilities in a test system to ensure they have a solution that will address these physical layer characterization test needs.

Solution

A vector network analyzer (VNA) can provide complete characterization of complex microwave behavior seen in high speed digital interconnects. A VNA's measurement of the input differential insertion loss, which indicates the frequency response the differential signal sees as it propagates through the high-speed serial channel, is required by many standards including Serial ATA and PCI Express ®.

A possible test solution consists of a PXI VNA and software optimized for physical layer test. The hardware and software can automate programming of test sequences for full characterization of high speed digital devices regardless of the domain and analysis format selected by the designer. A PXI vector network analyzer achieves fast measurement speed required in high-volume production test in a small modular form factor needed in a manufacturing test environment. This flexible and easy to use system must address the need for both time and frequency domain analysis at higher data rates. In order to accommodate increasing data rates, the physical layer test system must have the ability to apply eye diagrams for statistical analysis and translation of the device performance into standards compliance. The resulting eye diagram characterization is also valuable for optimal simulations and measurement-based s-parameters.

Keysight developed a test system designed specifically for signal integrity analysis called the Physical Layer Test System (PLTS) 2017, which provides data collection and analysis software for frequency and time domain data along with instrument control. The PLTS 2017 uses efficient, SCPI command based automated testing with a 32-channel PXI vector network analyzer (VNA) that can execute a fully crossbar calibrated 32-port S-parameter measurement in only 10 to 15 seconds.

Physical layer test of high-speed digital designs can be a time consuming and challenging process. Engineers armed with an understanding of the fundamental properties of signal propagation during measurement and analysis, and a flexible, fully capable test solution will be able to address the increasing challenges high-speed interconnect test.

To learn more about addressing the challenges of today's Physical Layer test:
http://literature.cdn.keysight.com/litweb/pdf/5989-6841EN.pdf?id=1239572