

PXI Overview

By Michael Dewey, Marvin Test Solutions

The PCI eXtensions for Instrumentation (PXI) standard has quickly gained adoption and grown in prevalence in automated test systems since its release in 1998. Today, PXI is being selected as the test platform of choice for thousands of applications for a wide range of markets including military, aerospace, consumer electronics, communications, semiconductor, and transportation as well as process control and industrial automation. One of the key elements driving the rapid adoption of PXI is the use of PCI as its communication backplane.

As the commercial PC industry drastically improves the available bus bandwidth by transitioning PCI to PCI Express, PXI has the ability to address even more applications by integrating PCI Express into the PXI standard. Both the PCI Industrial Manufacturers Group (PICMG) which governs CompactPCI, and the PXI Systems Alliance (PXISA) which governs PXI, have worked to ensure that the PCI Express technology can be integrated into these standards, while preserving compatibility with the large installed base of existing systems. With PXI Express, users benefit from significantly increased bandwidth, ensured backward compatibility, and additional timing and synchronization features; improving upon an already established platform.

This document answers frequently asked questions about PXI Express.

General Concept of PXI Express

What is PXI Express?

PXI Express technology is the latest addition to the PXI platform. The PXI Express specification integrates PCI Express signaling into the PXI standard. This increases backplane bandwidth from 132 MB/s to 6 GB/s, a 45 times improvement. It also enhances PXI timing and synchronization features by incorporating a 100 MHz differential reference clock and differential trigger lines. The PXI Express specification adds these features to PXI while maintaining backwards compatibility with the PXI standard.

How does PXI Express compare to other buses in bandwidth and latency?

Bandwidth is the rate at which data is sent across a bus, expressed in megabytes per second; latency is the delay in transmission of data across a bus. With PXI Express,

you can achieve a maximum 6 GB/s controller-to-backplane bandwidth, the highest bandwidth in the test and measurement industry. Additionally, up to 2 GB/s of bandwidth can be dedicated to each peripheral slot, depending on the system specifics.

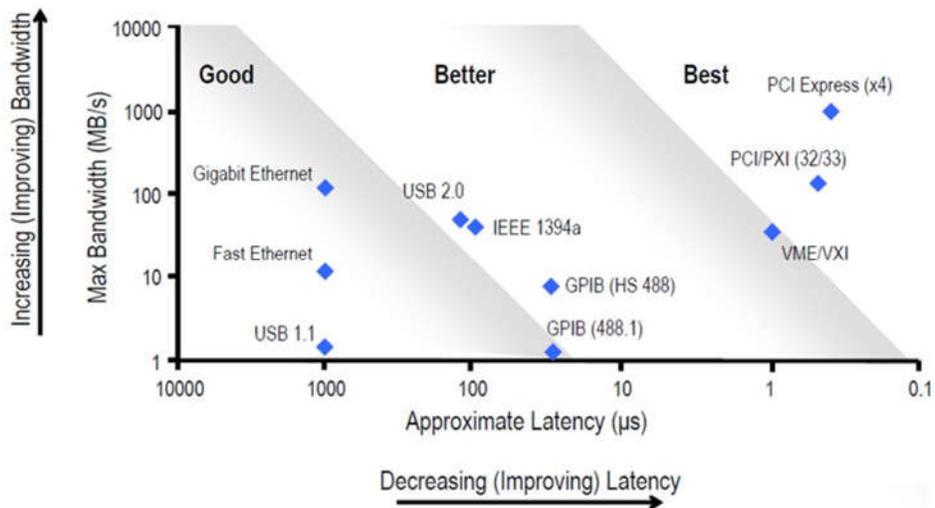


Figure 1. PXI Express provides the highest bandwidth and lowest latency in the test and measurement industry.

PXI Express offers the lowest latency of all mainstream commercial test and measurement bus technologies, delivering latency comparable to – and in some cases better than – PCI-based PXI. Also, PXI Express latency is several orders of magnitude better than the latencies of external buses such as USB or Ethernet.

How Does PXI Express take advantage of the PCI Express 2.0 specification?

In January 2007, PCI Special Interest Group (PCI-SIG) announced the PCI Express 2.0 specification which doubles the per-lane throughput from 250 MB/s to 500 MB/s. This means a 32-lane PCI connector (x32) can support throughput up to 16 GB/s aggregate, and the specification is backwards compatible with the previous PCI Express implementation.

PXI Express does take advantage of PCI Express advancements. The PCI Express 2.0 specification gives PXI Express the ability to continue to provide bandwidth improvements for PXI users. Embedded controllers are now available that offer four x4 Gen 2 PCI Express links for interfacing to the PXI chassis backplane. And when used in conjunction with a PXI Express chassis, total system data throughput of 8 GB/s can be supported. With this capability, you can simultaneously stream a larger set of I/O channels, giving you the ability to support larger and more complex data record-and-playback applications.

PCI-SIG continues to evolve the PCI Express standard and is currently working on the PCI Express 3.0 specification, which will continue to improve the bandwidth capabilities.

What are the different types of slots in a PXI Express chassis?

A PXI Express chassis can include the following:

- A system slot, which accepts an embedded or remote PXI Express controller
- PXI peripheral slots, which accept PXI modules
- PXI Express hybrid peripheral slots, which accept PXI Express peripheral modules, 32-bit CompactPCI peripheral modules, and hybrid-compatible PXI peripheral modules
- A system timing slot, which accepts both PXI Express peripheral modules and PXI Express system timing modules

Figure 2 shows a PXI backplane which supports the various PXI slots listed above

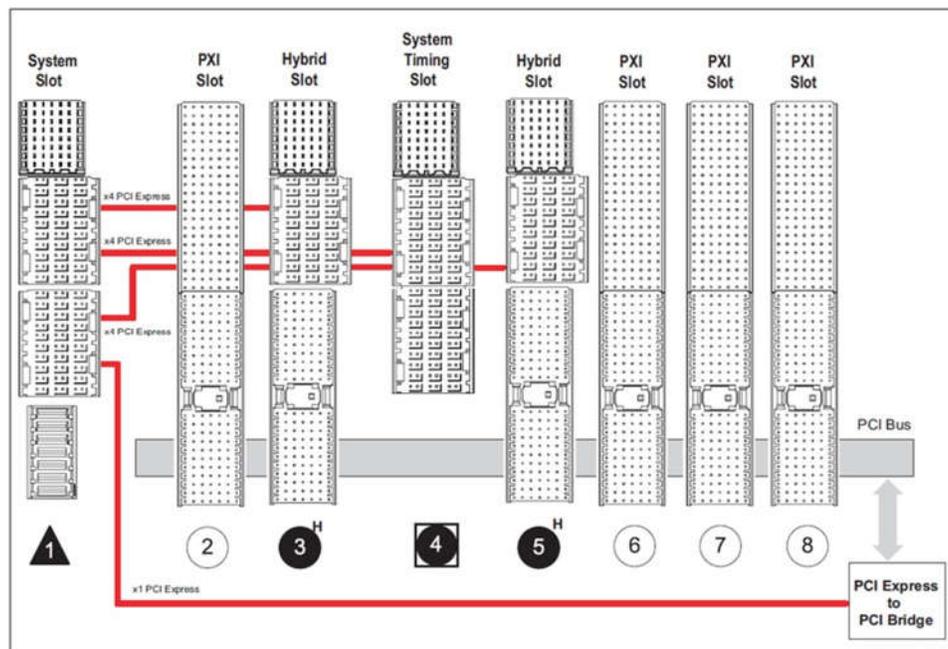


Figure 2. The backplane layout for a PXI Express chassis which comprises multiple slots

Does PXI Express replace PXI?

No. PXI Express is part of the PXI platform, and PXI vendors continue to invest in both platforms by developing products that are based on both PCI and PCI Express signaling. Many applications, including general data acquisition and motion control, do not require the increased bandwidth of PXI Express, so you need to choose which specification within the PXI platform is right for you. PXI systems already serve a large installed base of applications, and PXI systems based on PCI signaling will be deployed

in large numbers for many years to come. Additionally, suppliers of PXI Express chassis include both PXI peripheral slots and PXI Express hybrid peripheral slots, allowing users to incorporate both PXI peripheral modules and PXI Express peripheral modules together in the same chassis and system.

Is PXI Express backwards compatible with PXI?

Yes. PXI Express maintains both software and hardware compatibility with PXI peripheral modules.

Software: PCI Express uses the same OS and driver model as PCI, resulting in complete software compatibility between PCI-based systems (such as PXI) and PCI Express-based systems (such as PXI Express). This software compatibility is ensured by the PCI-SIG, a group composed of member companies who are committed to the development and enhancement of the PCI and PCI Express standards.

Hardware: PXI Express chassis provide hybrid peripheral slots that accept PXI Express peripheral modules and hybrid slot-compatible PXI peripheral modules. These peripheral slots deliver signaling for PCI and PCI Express.

Can I use my existing code written for previous PXI systems?

Yes. PXI Express maintains complete software compatibility with PXI. Software compatibility includes operating systems such as Windows 10 and Linux®, application software such as Microsoft Office and other Windows-based APIs.

What is a PXI Express hybrid slot?

PXI Express chassis have two kinds of peripheral slots: PXI peripheral slots and PXI Express hybrid peripheral slots. The PXI hybrid peripheral slots, shown in Figure 3, can accept either PXI Express peripheral modules, 32-bit CompactPCI boards, or hybrid slot-compatible PXI modules.

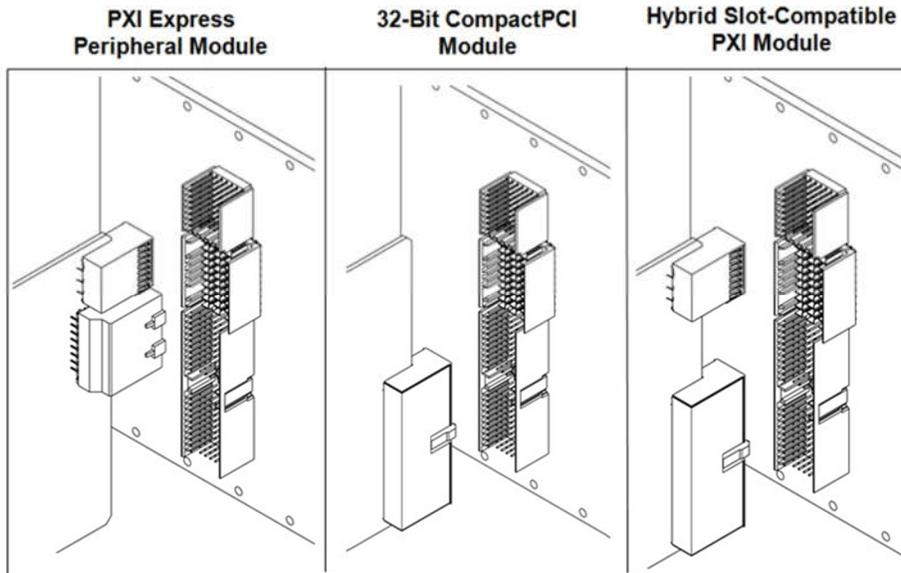
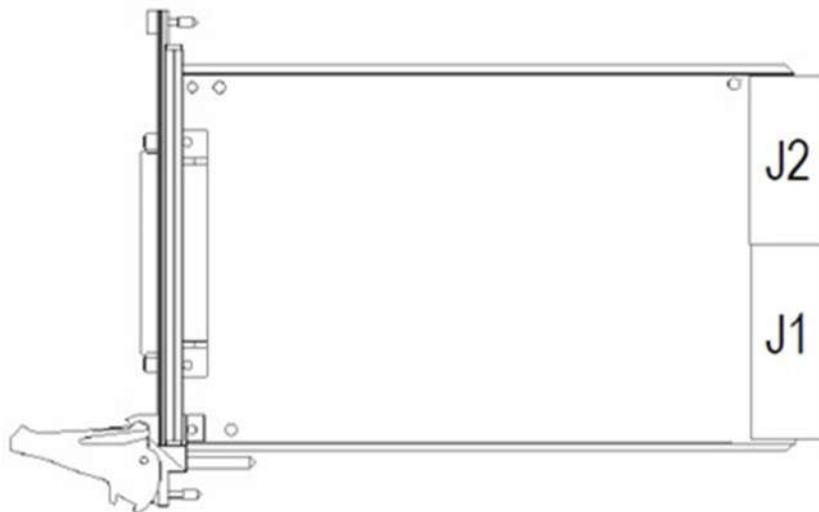


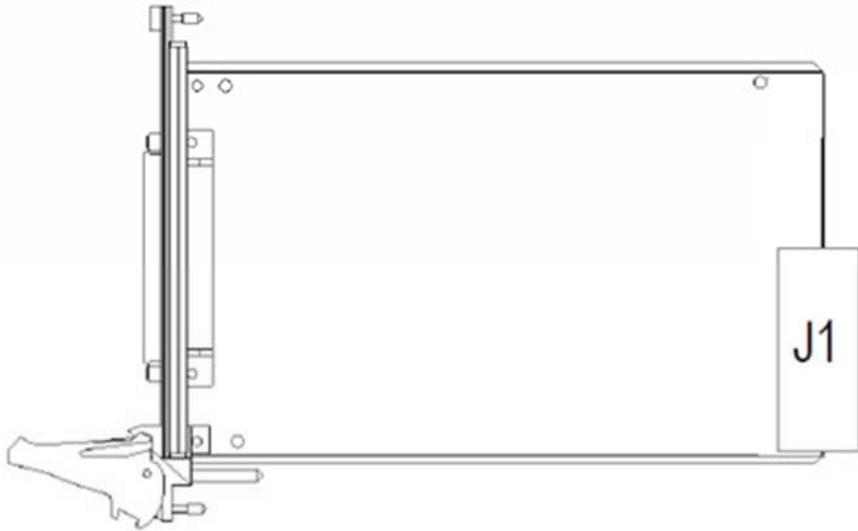
Figure 3. A PXI Express hybrid slot accepts PXI Express peripheral modules, 32-bit CompactPCI boards, and hybrid slot-compatible PXI modules.

What is a hybrid slot-compatible PXI module?

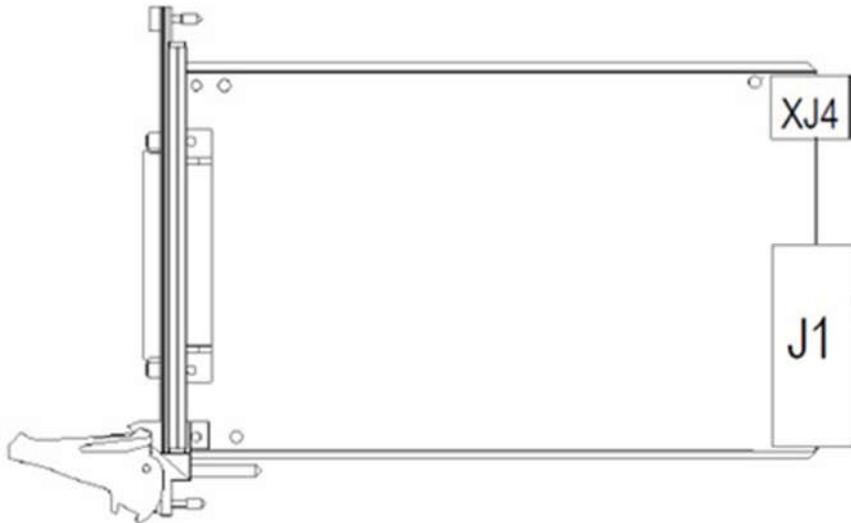
PXI modules that do not include a J2 connector are already hybrid slot-compatible. For modules that do include the J2 connector, you must replace that physical connector to achieve compatibility with PXI Express hybrid peripheral slots. As shown in Steps 1 through 3 below, the J2 connector is removed and replaced with the smaller eHM connector (XJ4). You can still use the resulting hybrid slot-compatible module in existing PXI peripheral slots.



Step 1. Select a PXI peripheral module that you would like to modify.



Step 2. Depopulate the J2 connector.



Step 3. Populate the eHM (XJ4) connector.

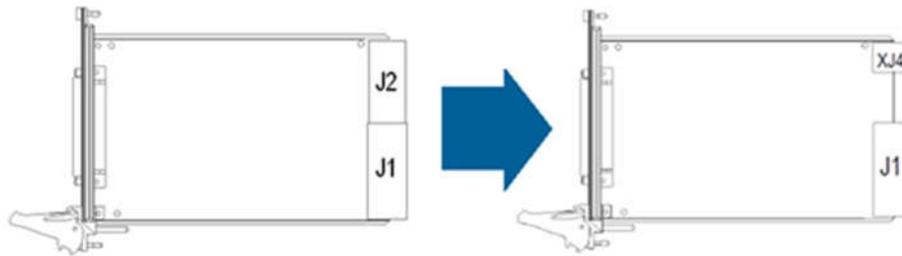


Figure 4. Connector Modification of a PCI-Based PXI Module for Hybrid Slot Compatibility

In general, modified modules only require replacement of the backplane connector, the rest of the module is unchanged. This modification takes advantage of the fact that the lower portion of the J2 connector is largely unused in 32-bit PXI modules, with the exception of its use for local bus functionality.

What happens to my existing PXI equipment?

You can use existing PXI peripheral modules in PXI Express chassis that have hybrid slots and in PXI chassis. Because the PXI Express specification offers a feature set enhancement and not a replacement for PXI, PXI vendors will continue to develop and sell PXI controllers, chassis, and modules based on PCI signaling.

To use existing PXI peripheral modules in a PXI Express chassis, simply insert the module into one of the several PXI peripheral slots. If the existing equipment does not have a J2 connector, you also can place the module in a hybrid slot. If there are more existing PXI modules that have J2 connectors than there are PXI slots available, the remaining PXI modules can be converted to a hybrid slot compatible configuration.

Is there a comparable specification for CompactPCI based on PCI Express signaling?

Yes. The CompactPCI Express specification, upon which PXI Express was built, was released in June 2005. The specification is owned and maintained by the PCI Industrial Computer Manufacturers Group (PICMG).

What does x1, x4, and x16 mean?

With PCI Express, data is sent serially through pairs of transmit and receive connections called lanes, which give data the ability transfer at 250 MB/s per direction. Multiple lanes can be grouped together into x1 (“by-one”), x2, x4, x8, x12, x16, and x32

links to increase bandwidth to the slot. For example, a x16 slot would have bandwidth of 4 GB/s per direction (250 MB/s * 16).

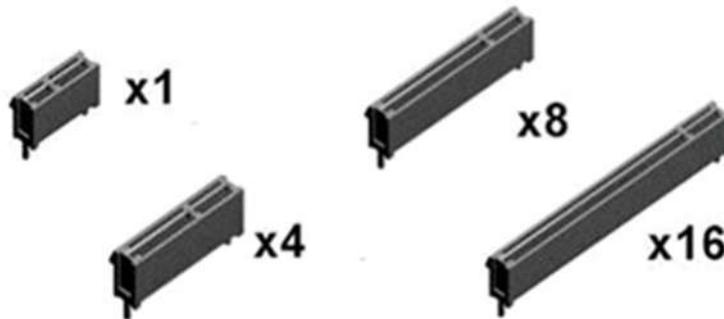


Figure 5. These examples show the various PCI Express connectors.

Though different lane widths correspond to different physical slot sizes in PCI Express, (Figure 5) PXI Express slots and connections do not differ physically based on the lane width of the link.

Does every PXI Express slot necessarily have its own dedicated bandwidth?

The answer depends on the implementation of the PCI Express bus in the chassis and controller. If the PCI Express lanes for the slot are directly linked to the controller chipset, then the slot has its own dedicated bandwidth. But if the controller and/or chassis use a PCI Express switch to split the link so that it fans out to several slots, those slots share the bandwidth.

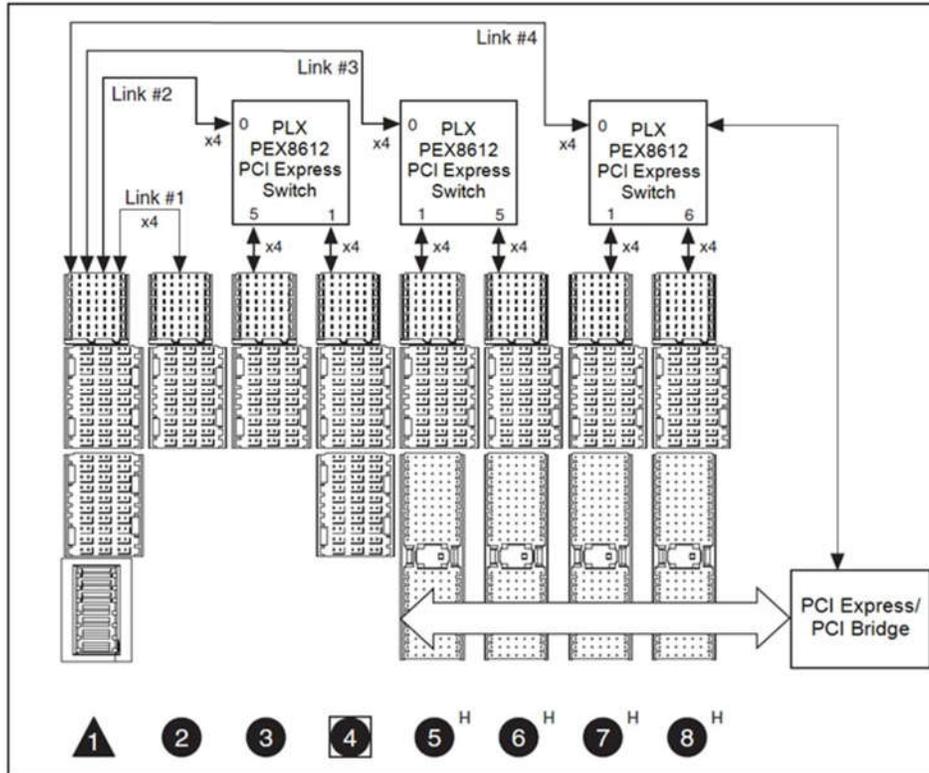


Figure 6. Backplane architecture shows the PXI Express slot bandwidth capabilities.

In Figure 6 above, the PXI Express chassis has four x4 links that connect the controller slot to the backplane. Slot 2 of the chassis would have dedicated bandwidth back to the controller because it does not require a switch. However, slots 3 and 4 of the chassis route through a switch on the backplane which connectors to a x4 link back to the controller. Because slots 3 and 4 go through a switch, they share bandwidth. Similarly, slots 5 and 6, along with 7 and 8, also use a switch and therefore share the bandwidth of the x4 link back to the controller.

How is local bus affected?

The PXI local bus provides a daisy-chained connection between each PXI peripheral slot and the adjacent PXI peripheral slots to its left and right. With the exception of a single local bus pin, local bus is not available in the PXI Express hybrid slots or on PXI Express modules. The physical connector space previously used by local bus is now occupied by a connector for PCI Express signaling. Local bus is, however, still available between adjacent PXI slots in the PXI Express chassis and will continue to be available in the future PCI-based PXI chassis.

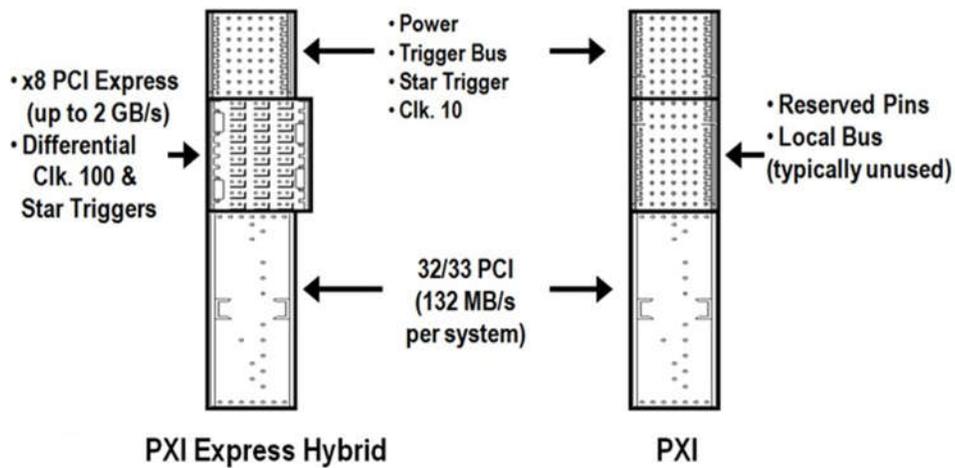


Figure 7. A PXI Express hybrid slot provides compatibility with PXI modules with PCI signaling and will work with future PXI Express modules with PCI Express signaling.

Summary

The PXI Express standard expands the capabilities and performance of the PXI architecture by leveraging the PCI Express specification while preserving compatibility with the PXI standard. In addition, PXI Express maintains complete software compatibility with PXI, allowing users to easily transition applications from PXI to PXI Express platforms.

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