PXI™-6

PXI Express Software Specification

PCI EXPRESS eXtensions for Instrumentation

An Implementation of *CompactPCI® Express*

Revision 1.0
August 31, 2005

PXI Systems Alliance

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PXI Express Software Specification Revision History

This section is an overview of the revision history of the PXI Express Software Specification.

Revision 1.0, August 31, 2005

This is the first public revision of the PXI Express Software Specification.

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1. Introduction

This section explains the objectives and scope of the *PXI Express Software Specification*. It also describes the intended audience and lists relevant terminology and documents. Note that this specification is intended to supplement the *PXI Express Hardware Specification*. Refer to the *PXI Express Hardware Specification* for general background on PXI and its electrical and mechanical requirements.

1.1 Objectives

The *PXI Express Software Specification* was created to provide a standard for software support of the new features introduced by the *PXI Express Hardware Specification*. PXI Express brings a rich set of new module types and backplane features. The software specification's purposes are to describe the capabilities of PXI Express hardware components using standard hardware description files and to promote interoperability among PXI Express vendors with respect to software requirements. The software specification addresses a variety of issues, including hardware description, hardware resource management, operating system framework definition, and the incorporation of existing instrumentation software standards.

There are three major objectives for the *PXI Express Software Specification*. The first objective is to define a set of software interfaces for characterizing PXI Express components and their capabilities. The scope of this objective is wider than in previous PXI software specifications. This wider scope is intended to accommodate the powerful new features provided by the *PXI Express Hardware Specification* for PXI Express components, including Chassis self-identification, geographical addressing, and an SMBus. Interfaces in previous PXI Specifications have become more flexible. For example, while PXI-1 controllers had one PCI bus communicating with the PXI backplane, PXI Express controllers will have two or four PCI Express links communicating to the backplane. Each of those links may be routed to the switch fabric with considerable flexibility. In such a flexible system, it becomes necessary for peripheral software components to be responsible for discovering their own device locations, instead of requiring a central resource manager to infer that information from static Chassis description files. As such, the *PXI Express Software Specification* defines requirements for APIs to be implemented by the module vendor and the controller vendor. The specification also defines file formats, component registration mechanisms, and binary linkage to ensure interoperability of these components.

The second objective of this specification is compatibility with previous PXI software specifications. Despite the introduction of a new software architecture, the system description files generated by the resource manager will comply with the *PXI Software Specification*. All software interacting with PXI-1 modules in PXI-1 slots or hybrid slots will continue to function without modification. Additionally, the new module APIs defined in this specification are designed so that they can be implemented independently of the instrument drivers for those modules.

The third objective of this specification is to define standard operating system frameworks and to incorporate existing instrumentation software standards. Additional software requirements include the support of standard operating system frameworks such as Windows 2000 and Windows XP, and the support of instrumentation software standards developed by the VXI*plug&play* Systems Alliance (VISA).

1.2 Intended Audience and Scope

This specification is primarily intended for product developers interested in implementing and leveraging software features of the PXI Express platform. Hardware developers will be interested in using these software interfaces for identifying and describing the capabilities of PXI Express hardware products such as Chassis and system controller modules. Likewise, software developers and systems integrators should take advantage of these software interfaces to manage PXI Express resources, including triggers and the local bus, and to implement features such as slot identification and Chassis identification. Additionally, product developers and systems integrators should reference the operating system framework definitions to ensure system-level interoperability.

1.3 Background and Terminology

This section defines the acronyms and key words referred to throughout this specification. This specification uses the following acronyms:

- **API—**Application Programming Interface
- **CompactPCI**—PICMG 2.0 Specification
- **PCI—**Peripheral Component Interconnect; electrical specification defined by PCISIG
- **PCISIG—**PCI Special Interest Group
- **PICMG—**PCI Industrial Computer Manufacturers Group
- **PXI—**PCI eXtensions for Instrumentation
- **VISA—**Virtual Instrument Software Architecture
- **VPP—**VXI*plug&play* Specification

This specification uses several key words, which are defined as follows:

RULE: Rules SHALL be followed to ensure compatibility. A rule is characterized by the use of the words SHALL and SHALL NOT.

RECOMMENDATION: Recommendations consist of advice to implementers that will affect the usability of the final module. A recommendation is characterized by the use of the words SHOULD and SHOULD NOT.

PERMISSION: Permissions clarify the areas of the specification that are not specifically prohibited. Permissions reassure the reader that a certain approach is acceptable and will cause no problems. A permission is characterized by the use of the word MAY.

OBSERVATION: Observations spell out implications of rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules, so that the reader understands why the rule must be followed.

MAY: A key word indicating flexibility of choice with no implied preference. This word is usually associated with a permission.

SHALL: A key word indicating a mandatory requirement. Designers SHALL implement such mandatory requirements to ensure interchangeability and to claim conformance with the specification. This word is usually associated with a rule.

SHOULD: A key word indicating flexibility of choice with a strongly preferred implementation. This word is usually associated with a recommendation.

1.4 Applicable Documents

This specification defines extensions to the base PCI and CompactPCI specifications referenced in this section. It is assumed that the reader has a thorough understanding of PCI and CompactPCI. The CompactPCI specification refers to several other applicable documents with which the reader may want to become familiar. This specification refers to the following documents directly:

- *PXI-1: PXI Hardware Specification,* Rev. 2.2
- *PXI-3: VISA for PXI Specification,* Rev. 1.0
- *PXI-4: PXI Module Description File Specification,* Rev. 1.0
- *PXI-5: PXI Express Hardware Specification,* Rev. 1.0

- *PCI Local Bus Specification*, Rev. 2.2
- *PICMG 2.0 R3.0 CompactPCI Specification*
- *PICMG EXP.0 R1.0 CompactPCI Express Specification*

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2. Hardware Description Files

This section defines the formats of the hardware description files and describes their use.

2.1 System Description Files

System description files describe PXI Express systems and their components. The system module and one or more PXI Chassis that comprise a PXI Express system determine a system description. A system description enables a variety of software functionality, including geographic slot identification and trigger routing. Chassis description files, from which much of the system description content is derived, are discussed later in this section.

2.1.1 System Description Definitions

To develop a system description, it is useful to define descriptors for the following PXI Express system components:

- **System**—A PXI Express System descriptor corresponds to a physical PXI Express system. A PXI Express System is a collection of Chassis. Multiple Chassis in a system are coupled in a software-transparent manner (that is, they are coupled via PCI Express switches and other PCI-PCI bridging).
  - **Chassis**—A Chassis descriptor corresponds to a physical PXI Chassis in a system. Chassis can include trigger buses, system timing sets, star triggers, and slots.
    - **Trigger Buses**—A PXI trigger bus descriptor corresponds to a physical trigger bus in a Chassis. A trigger bus is characterized by a list of slots sharing the physical trigger bus connection. Chassis can contain multiple trigger buses.
    - **Star System Timing Sets**—A star system timing set descriptor corresponds to the set of system timing sets contained in a PXI Express Chassis. The system timing sets for a Chassis are characterized by the system timing slot number and a mapping of system timing sets to peripheral slot numbers. A Chassis can contain multiple system timing sets.
    - **Star Triggers**—A PXI star trigger descriptor corresponds to a physical set of star triggers in a Chassis. A set of star triggers is characterized by a star trigger controller slot number and a mapping of PXI_STAR lines (defined in the *PXI Hardware Specification*) to peripheral slot numbers. A Chassis can contain multiple sets of star triggers.
    - **Slots**—A PXI slot descriptor corresponds to a physical slot in a Chassis. A slot is characterized by a geographic address, a PCI logical address, local bus routings, and other special capabilities. A Chassis has multiple slots.

In addition, a *Resource Manager* is defined as the entity responsible for creating a PXI Express system description file. For example, the responsibilities of a Resource Manager might be accomplished by a systems integrator, or a software utility might be provided to automate the Resource Manager algorithm.

RULE: A system module manufacturer SHALL provide either a system description file for each supported system configuration or a Resource Manager utility that can manage the system description file.

RECOMMENDATION: A system module manufacturer SHOULD provide a utility that can automate the Resource Manager algorithm.

RULE: A system description file SHALL be named `pxiesys.ini`. Refer to the Section 4, *Software Frameworks and Requirements*, to determine the location of the `pxiesys.ini` file for a given OS platform.

RECOMMENDATION: To aid systems integrators and operators, PXI Express module configuration and driver software SHOULD use geographic addressing information, available in a PXI Express system description file, to present Chassis and slot locations for PXI Express modules via a user interface.

2.1.2 System Descriptor

The system descriptor contains highest-level information about a PXI Express system. PXI Express systems are characterized by the Chassis that comprise the system, and the system descriptor contains a list of these Chassis.

RULE: A system description file SHALL contain one and only one system descriptor.

RULE: The system descriptor `.ini` section header SHALL be named "System."

RULE: Each system descriptor section SHALL contain one of each tag line types described in Table 2-1.

Table 2-1. System Description File—System Tag Line Descriptions

Tag	Valid Values	Description
ChassisList	A comma-separated list of *n*, where *n* is a decimal integer such that *n* >= 1.	This tag enumerates the Chassis in a PXI Express system.

System Descriptor Example

```
# This section describes a PXI Express system with two chassis.
[System]
ChassisList = 1,2
```

RULE: A Resource Manager SHALL derive the ChassisList tag value using the algorithm described in Section 3.5.

RULE: Multiple Chassis SHALL be uniquely numbered in the ChassisList tag.

OBSERVATION: Chassis can be numbered in an arbitrary fashion. For example, Chassis can be numbered according to their order of discovery using a depth-first PCI traversal algorithm.

2.1.3 Chassis Descriptor

A Chassis descriptor provides a high-level description of an individual PXI Express Chassis in a system. A Chassis descriptor contains collections of the components that comprise a Chassis, including trigger buses, system timing sets, sets of star triggers, and slots.

RULE: A system description file SHALL contain a distinct Chassis descriptor for each physical Chassis that comprises the PXI Express system.

OBSERVATION: Chassis are enumerated using a system descriptor's ChassisList tag.

RULE: A Chassis descriptor SHALL be named "Chassis*N*," where *N* is the Chassis number.

RULE: A Resource Manager SHALL derive Chassis numbers from the ChassisList tag of a system descriptor (see Table 2-1).

RECOMMENDATION: The Chassis number SHOULD be physically viewable on a Chassis to assist operators in locating Peripheral Modules.

RULE: Each Chassis descriptor SHALL contain one of each of tag line type described in Table 2-2.

Table 2-2. System Description File—Chassis Tag Line Descriptions

Tag	Valid Values	Description
Model	A string indicating the model name for this Chassis.	This tag identifies a Chassis model name.
Vendor	A string indicating the vendor name for this Chassis.	This tag identifies a Chassis vendor name.
SerialNumber	A 13-byte string specifying the backplane serial number.	Refer to the CompactPCI Express specification for details regarding the format of the serial number.
SlotList	A comma-separated list of *n*, where *n* is a decimal integer such that *n* >= 1.	This tag enumerates the slots in a Chassis.
TriggerBusList	A comma-separated list of *n*, where *n* is a decimal integer such that *n* >= 1.	This tag enumerates the trigger buses in a Chassis.
StarSystemTimingSetList	A comma-separated list of *n*, where *n* is a decimal integer such that *n* >= 1.	This tag enumerates the PXI Express system timing sets in a Chassis.
StarTriggerList	A comma-separated list of *n*, where *n* is a decimal integer such that *n* >= 1.	This tag enumerates the sets of star triggers in a Chassis.

Chassis Descriptor Example

```
# This example describe an 8-slot PXI Express chassis with two
# peripheral slots (slots 2-3), four hybrid slots (slots 4-7), and
# one PXI-1 slot (slots 8).
[Chassis1]
Model = "Example 8-Slot Chassis"
Vendor = "Example Chassis Vendor"
SerialNumber = "000038a2e941"
SlotList = 1,2,3,4,5,6,7,8
TriggerBusList = 1
StarSystemTimingSetList = 1
StarTriggerList = 1
```

RULE: A Resource Manager SHALL derive the nonshaded tag values in Table 2-2 from the tag values of the corresponding Chassis description file's Chassis descriptor (see Table 2-10).

RULE: A Resource Manager SHALL derive the SerialNumber tag value using the Chassis EEPROM, accessed via the System Module Driver interface described in Section 3.3.1, *System Module Drivers*.

2.1.4 Trigger Bus Descriptor

A trigger bus descriptor describes an individual trigger bus in a PXI Express Chassis. A trigger bus is characterized by a list of slots that reside on the trigger bus.

RULE: A system description file SHALL contain a distinct PXI Express trigger bus descriptor for each physical PXI trigger bus in the system.

RULE: A trigger bus descriptor SHALL be named "Chassis*M*TriggerBus*N*," where *M* is the Chassis number and *N* is the trigger bus number.

RULE: A Resource Manager SHALL derive trigger bus numbers from the TriggerBusList tag of the corresponding Chassis descriptor (see Table 2-2).

OBSERVATION: While each trigger bus number will uniquely correspond to a set of PXI Express slots, there is not necessarily a one-to-one correspondence between trigger buses and PCI bus segments.

RULE: Each trigger bus descriptor SHALL contain one of each of the tag line types described in Table 2-3.

Table 2-3. System Description File—Trigger Bus Tag Line Descriptions

Tag	Valid Values	Description
SlotList	A comma-separated list of *n*, where *n* is a decimal integer such that *n* >= 1.	This tag enumerates the slots on a trigger bus.

Trigger Bus Descriptor Example

```
# This example describe an 8-slot PXI Express chassis with two
# peripheral slots (slots 2-3), four hybrid slots (slots 4-7), and
# one PXI-1 slot (slots 8).
# The trigger bus spans each of the eight slots.
[Chassis1TriggerBus1]
SlotList = 1,2,3,4,5,6,7,8
```

RULE: A Resource Manager SHALL derive the tag values in Table 2-3 from the tag values of the corresponding Chassis description file's Trigger Bus descriptor (see Table 2-11).

2.1.5 Star System Timing Sets Descriptor

A star system timing sets descriptor describes the system timing sets in a PXI Express Chassis. A star system timing sets descriptor is characterized by a system timing slot number and a mapping of system timing sets (that is, PXIe_DSTARA*n*, PXIe_DSTARB*n*, and PXIe_DSTARC*n*) to peripheral slot numbers.

RULE: A system description file SHALL contain a distinct star system timing sets descriptor for each system timing slot in the system.

RULE: A star system timing sets descriptor SHALL be named "*ChassisMStarSystemTimingSetsN*," where *M* is the Chassis number and *N* is the number for the system timing sets.

RULE: A Resource Manager SHALL derive star system timing sets descriptor numbers from the StarSystemTimingSetsList tag of the corresponding Chassis descriptor (see Table 2-2).

RULE: A star system timing sets descriptor SHALL contain one of each of the tag line types described in Table 2-4.

Table 2-4. System Description File—Star System Timing Sets Tag Line Descriptions

Tag	Valid Values	Description
SystemTimingSlot	A decimal integer *n*, where *n* is a decimal integer such that *n* >= 1.	This tag specifies the slot number of the system timing slot for this group of system timing sets.
StarSystemTimingSet*n* (where *n* is a decimal integer such that 0 <= *n* <= 16), for each possible system timing set for a given system timing module.	A comma-separated list of *m*, where *m* is a decimal integer, corresponding to a PXI slot number, such that *m* >= 1.	This tag specifies the peripheral slot number corresponding to a set of PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC lines.

Star System Timing Sets Descriptor Example

```
# This example describe an 8-slot PXI Express chassis with two
# peripheral module slots (2-3), four hybrid slots (4-7), and one
# PXI-1 slot (8).
# The system timing set controller slot is slot 4, and the system
# timing set mapping to each hybrid peripheral slot is described.
[Chassis1StarSystemTimingSet1]
SystemTimingSlot = 4
SystemTimingSet0 = 4
SystemTimingSet1 = 2
SystemTimingSet2 = 3
SystemTimingSet3 = 5
SystemTimingSet4 = 6
SystemTimingSet5 = 7
```

RULE: A Resource Manager SHALL derive the tag values in Table 2-4 from the tag values of the corresponding Chassis description file's star system timing sets descriptor (see Table 2-13).

OBSERVATION: The star system timing sets descriptor allows configuration software to describe alternative system timing sets to slot mappings.

OBSERVATION: If a star system timing set is not routed to a PXI Express slot, the corresponding StarSystemTimingSets*n* tag will not be listed in the star system timing sets descriptor.

2.1.6 Star Trigger Descriptor

A star trigger descriptor describes an individual set of star triggers in a PXI Express Chassis. A star trigger descriptor is characterized by a star trigger controller slot number and a mapping of PXI_STAR lines, as defined in the *PXI Express Hardware Specification*, to peripheral slot numbers.

RULE: A system description file SHALL contain a distinct PXI star trigger descriptor for each physical set of PXI star triggers in the system.

RULE: A star trigger descriptor SHALL be named "Chassis*M*StarTrigger*N*," where *M* is the Chassis number and *N* is the number for the set of star triggers.

RULE: A Resource Manager SHALL derive star trigger descriptor numbers from the StarTriggerList tag of the corresponding Chassis descriptor (see Table 2-2).

RULE: Each star trigger descriptor SHALL contain one of each of the tag line types described in Table 2-5.

Table 2-5. System Description File—Star Trigger Tag Line Descriptions

Tag	Valid Values	Description
SystemTimingSlot	*n*, where *n* is a decimal integer such that *n* >= 1.	This tag specifies the star trigger controller slot number for a PXI_STAR lines in a set of star triggers.
PXI_STAR*n* (where *n* is a decimal integer such that 0 <= *n* <= 16), for each PXI star trigger line physically routed to a PXI slot	A comma-separated list of *m*, where *m* is a decimal integer, corresponding to a PXI slot number, such that *m* >= 1.	This tag specifies the PXI_STAR line to slot mapping for a set of star triggers.

Star Trigger Descriptor Example

```
# This example describes an 8-slot PXI Express chassis with two
# peripheral slots (slots 2-3), four hybrid slots (slots 4-7), and
# one PXI-1 slot (slots 8).
# The star trigger controller slot is slot 4.
[Chassis1StarTrigger1]
SystemTimingSlot = 4
PXI_STAR0 = 1
PXI_STAR1 = 2
PXI_STAR2 = 3
PXI_STAR3 = 5
PXI_STAR4 = 6
PXI_STAR5 = 7
PXI_STAR6 = 8
```

RULE: A Resource Manager SHALL derive the tag values in Table 2-5 from the tag values of the corresponding Chassis description file's Star Trigger descriptor (see Table 2-13).

OBSERVATION: The star trigger descriptor allows configuration software to describe alternative star trigger line mappings.

OBSERVATION: If a star trigger line is not routed to a PXI Express slot, the corresponding PXI_STAR*n* tag will not be listed in the star trigger bus descriptor.

2.1.7 Slot Descriptors

Slot descriptors describe slots in PXI Express Chassis. PXI Express defines several slot types, including the system slot, and several types of peripheral slots.

A PXI Express Chassis' identification EPROM describes the type of slot implemented for a given slot number. The System Description Files includes this slot type information to enable simplified access for application software. Refer to the PXI Express Hardware Specification for detailed information about the types of possible slots in a PXI Express Chassis.

The following System Slot type values are defined:

Table 2-6. System Description File—System Slot Type Enumerated Values

Valid Values	Description
"PXIeSystemSlot2Link"	This tag value indicates that the system slot routes two PCI Express links.
"PXIeSystemSlot4Link"	This tag value indicates that the system slot routes four PCI Express links.

The following Peripheral Slot type values are defined:

Table 2-7. System Description File—Peripheral Slot Type Enumerated Values

Valid Values	Description
"PXIePeripheralSlot"	The tag value indicates that the peripheral slot is a PXI Express peripheral slot.
"PXIeHybridSlot"	This tag value indicates that the peripheral slot is a PXI Express Hybrid slot.
"PXIeSystemTimingSlot"	This tag value indicates that the peripheral slot is a PXI Express System Timing slot.
"PXI-1Slot"	This tag value indicates that the peripheral slot is a PXI-1 slot.

2.1.7.1 System Slot Descriptor

A system slot descriptor describes the system slot in a PXI Express Chassis. A system slot descriptor is characterized by the features of the slot it describes, including manufacturer and model information for a module present in the slot, the type of Chassis slot, and PCI Express link widths for the backplane slot and peripheral module.

RULE: A system description file SHALL contain a single system slot descriptor for each physical system slot in the PXI Express system.

RULE: A system slot descriptor SHALL be named "Chassis*M*Slot*N*," where *M* is the Chassis number, and *N* is the physical slot number.

OBSERVATION: A PXI Express system slot will always be numbered 1 for a given Chassis. Refer to the *PXI Express Hardware Specification* for more information.

RULE: Each system slot descriptor SHALL contain one of each of tag line types described in Table 2-8.

Table 2-8. System Description File—System Slot Tag Line Descriptions

Tag	Valid Values	Description
Model	A string value.	This tag identifies the model name for the PXI Express system module residing in the slot.
Vendor	A string value.	This tag identifies the vendor name for the PXI Express system module residing in the slot.
ModelInstance	*n*, where *n* is a decimal integer such that *n* >= 1.	This tag specifies the unique instance number of the PXI Express system module residing in this slot for the PXI Express system.
SlotType	A string value corresponding to the enumerated values specified in Table 2-6.	This tag specifies the type of system slot.
SystemSlotLinkWidth1	*n*, where *n* is a decimal integer such that n = 1, 4, or 8.	This tag specifies the routed link width of the PCI Express Link Number 1 of the system slot.
SystemSlotLinkWidth2	*n*, where *n* is a decimal integer such that n = 1, 4, 8, or 16.	This tag specifies the routed link width of the PCI Express Link Number 2 of the system slot.
SystemSlotLinkWidth3	*n*, where *n* is a decimal integer such that n = 0, 1, 4.	This tag specifies the routed link width of the PCI Express Link Number 3 of the system slot.
SystemSlotLinkWidth4	*n*, where *n* is a decimal integer such that n = 0, 1, 4.	This tag specifies the routed link width of the PCI Express Link Number 4 of the system slot.
ControllerModuleLinkWidth1	*n*, where *n* is a decimal integer such that n = 1, 4, or 8.	This tag specifies the maximum link width of the PCI Express Link Number 1 of the system module.
ControllerModuleLinkWidth2	*n*, where *n* is a decimal integer such that n = 1, 4, 8, or 16.	This tag specifies the routed link width of the PCI Express Link Number 2 of the system module.
ControllerModuleLinkWidth3	*n*, where *n* is a decimal integer such that n = 0, 1, 4.	This tag specifies the routed link width of the PCI Express Link Number 3 of the system module.

ControllerModuleLinkWidth4	*n*, where *n* is a decimal integer such that n = 0, 1, 4.	This tag specifies the routed link width of the PCI Express Link Number 4 of the system module.

System Slot Descriptor Example

```
# This example describe an 8-slot PXI Express chassis with two
# peripheral slots (slots 2-3), four hybrid slots (slots 4-7), and
# one PXI-1 slot (slots 8).
[Chassis1Slot1]
Model = "Example PXI Express System Model"
Vendor = "Example PXI Express System Vendor"
SlotType = PXIeSystemSlot2Link
SystemSlotLinkWidth1 = 8
SystemSlotLinkWidth2 = 16
SystemSlotLinkWidth3 = 0
SystemSlotLinkWidth4 = 0
ControllerModuleLinkWidth1 = 1
ControllerModuleLinkWidth2 = 1
ControllerModuleLinkWidth3 = 0
ControllerModuleLinkWidth4 = 0
```

RULE: A Resource Manager SHALL derive the Model, Vendor, and ModelInstance tag values using the System Module Driver interfaces defined in Section 3.3.1.

RULE: A Resource Manager SHALL derive the SlotType and SystemSlotLinkWidth*n* tag values from the corresponding values in the PXI Express Chassis' configuration EPROM. Refer to the CompactPCI Express specification for complete discussion of a Chassis' backplane capability record.

OBSERVATION: A PXI Express chassis' EEPROM is accessed using the System Module Driver Interface defined in Section 3.3.1, *System Module Drivers*.

RULE: A PXI Express Resource Manager SHALL derive the ControllerModuleLinkWidth*n* tag values using the System Module Driver Interface defined in Section 3.3.1, *System Module Drivers*.

2.1.7.2 Peripheral Slot Descriptor

A peripheral slot descriptor describes an individual peripheral slot in a PXI Express Chassis. A peripheral slot descriptor is characterized by the features of the slot it describes, including routing information for the slot's local bus lines and the PCI logical address for a module that might occupy the slot.

RULE: A system description file SHALL contain a distinct peripheral slot descriptor for each physical peripheral slot in the PXI Express system.

RULE: A slot descriptor SHALL be named "Chassis*M*Slot*N*," where *M* is the Chassis number, and *N* is the physical slot number.

RULE: A Resource Manager SHALL derive peripheral slot numbers from the SlotList tag of the corresponding Chassis descriptor (see Table 2-2).

RULE: Each slot descriptor SHALL contain one of each of nonshaded tag line type described in Table 2-9.

Table 2-9. System Description File—Peripheral Slot Tag Line Descriptions

Tag	Valid Values	Description
Model	A string value.	This tag identifies the model name for the PXI Express peripheral module residing in the slot.
Vendor	A string value.	This tag identifies the vendor name for the PXI Express peripheral module residing in the slot.
ModelInstance	*n*, where *n* is a decimal integer such that *n* >= 1.	This tag specifies the unique instance number of the PXI Express module residing in this slot for the PXI Express system.
SlotType	A string value corresponding to the enumerated values specified in Table 2-7.	This tag specifies the type of PXI Express slot.
SystemSlotLinkOrigin1	*n*, where *n* is a decimal integer such that 0 <= *n* <= 4.	This tag specifies which System Slot Link Number this slot's Links are directly or indirectly (via Switch or Bridge) connected to.
SystemSlotLinkOrigin2	*n*, where *n* is a decimal integer such that 0 <= *n* <= 4.	This tag specifies which System Slot Link the Bridge originates from for Hybrid Slots and PXI-1 Slots.
PeripheralSlotLinkWidth1	*n*, where *n* is a decimal integer such that *n* = 0, 1, 4, or 8.	This tag specifies the routed link width of this slot's PCI Express Link Number 1.
PeripheralSlotLinkWidth2	*n*, where *n* is a decimal integer such that *n* = 0, 1, 4, 8, or 16.	This tag specifies the routed link width of this slot's PCI Express Link Number 2.
PeripheralModuleLinkWidthMax	*n*, where *n* is a decimal integer such that *n* = 0, 1, 4, 8, or 16.	This tag specifies the maximum link width supported by the peripheral module in this slot.
PeripheralModuleLinkWidthNegotiated	*n*, where *n* is a decimal integer such that *n* = 0, 1, 4, 8, or 16.	This tag specifies the actual negotiated link width for the peripheral module in this slot.

Peripheral Slot Descriptor Example

```
# This example describes Slot 4 of an 8-slot PXI Express chassis.
# The slot is a peripheral slot that connects to a PCI
# Express switch that originates from the system slot's Link #1.
```

```
# The link width is x4, and a x1 PXI Express module is present.
[Chassis1Slot4]
Model = "Example PXI Express Model"
Vendor = "Example PCI Express Vendor"
ModelInstance = 1
PCIBusNumber = 2
PCIDeviceNumber = 19
LocalBusLeft = None
LocalBusRight = Chassis1Slot5
SlotType = PXIePeripheralSlot
SystemSlotLinkOrigin1 = 1
SystemSlotLinkOrigin2 = 0
PeripheralSlotLinkWidth1 = 4
PeripheralSlotLinkWidth2 = 0
PeripheralModuleLinkWidthMax = 1
PeripheralModuleLinkWidthNegotiated = 1
```

RULE: A Resource Manager SHALL derive the Model, Vendor, and ModelInstance tag values using the Peripheral Module Driver interfaces described in Section 3.3.3.

RULE: A Resource Manager SHALL derive the SlotType, SystemSlotLinkOrigin*n,* and PeripheralSlotLinkWidth*n* tag values from the corresponding values in the PXI Express Chassis' configuration EPROM. Refer to the CompactPCI Express specification for complete discussion of a Chassis' backplane capability record.

OBSERVATION: A PXI Express chassis' EEPROM is accessed using the System Module Driver Interface defined in Section 3.3.1, *System Module Drivers*.

RULE: A PXI Express Resource Manager SHALL derive the PeripheralModuleLinkWidthMax and PeripheralModuleLinkWidthNegotiated tag values using the Peripheral Module Driver Interface defined in Section 3.3.1, *System Module Drivers*.

2.1.8 System Description File Example

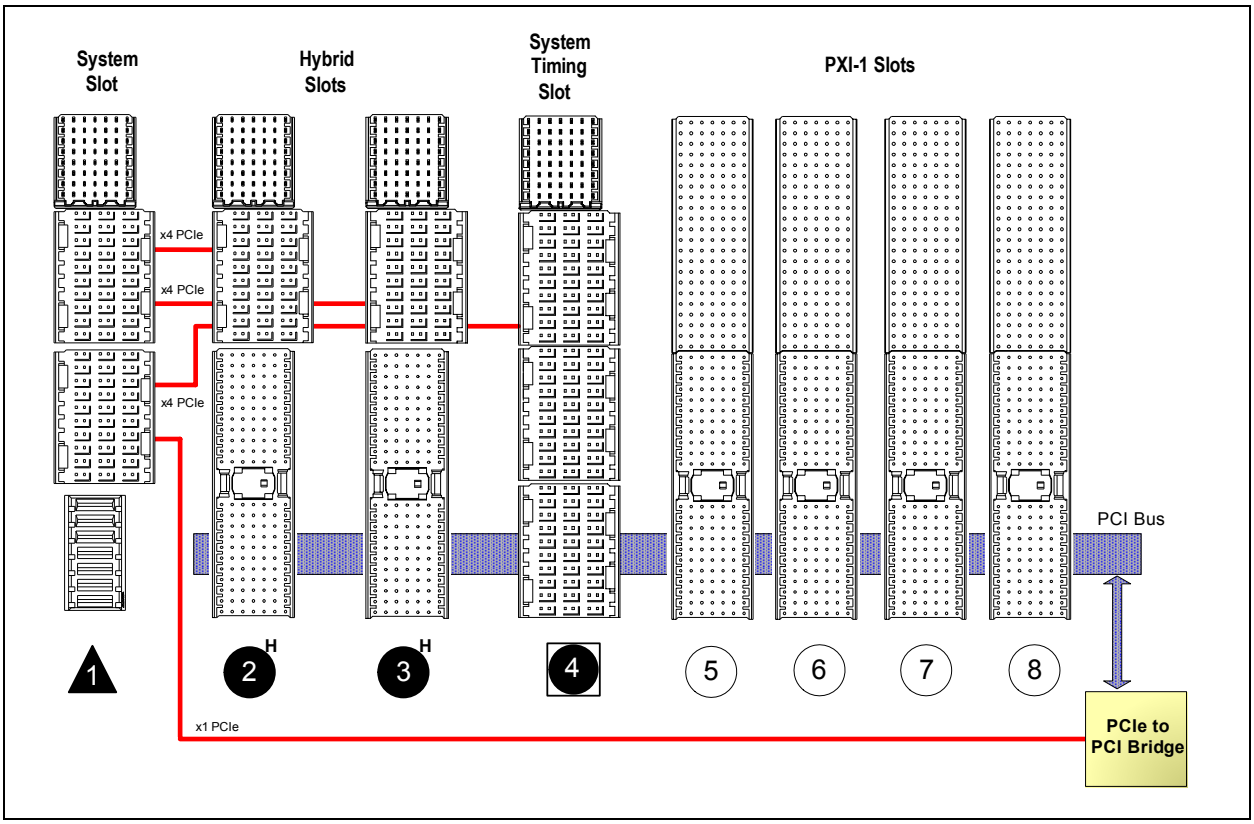
The following is a complete example of a PXI Express System Description file.

2.1.8.1 Single-Chassis PXI Express System

The following example system includes a single PXI Express Chassis. The Chassis described includes peripheral slots, hybrid slots, and a single PXI-1 slot. In addition, the Chassis includes modules in each slot.

The PXI Express Chassis includes a 4-link system controller slot (slot 1), two hybrid slots (slots 2-3), a system timing slot (slot 4), and four PXI-1 slots (slots 5-8). The backplane is a 4-link configuration, routing link 1 to slot 2, link 2 to slot 3, link 3 to slot 4, and link 4 to a PCIe-to-PCI bridge that forms that bus for the hybrid and legacy slots.

Refer to the following figure for a graphical representation of the PXI Express backplane in this system.




```
# This section describes a PXI Express system with one 8-slot chassis.
[System]
ChassisList = 1

[Chassis1]
Model = "Example 8-Slot Chassis"
Vendor = "Example Chassis Vendor"
SerialNumber = "000038a2e941"
SlotList = 1,2,3,4,5,6,7,8
TriggerBusList = 1
StarSystemTimingSetList = 1
StarTriggerList = 1

# The trigger bus spans each of the eight slots.
[Chassis1TriggerBus1]
SlotList = 1,2,3,4,5,6,7,8

# The system timing slot is slot 4, and the system
# timing set mapping to each hybrid peripheral slot is described.
[Chassis1StarSystemTimingSet1]
SystemTimingSlot = 4
SystemTimingSet0 = 4
SystemTimingSet1 = 2
SystemTimingSet2 = 3

[Chassis1StarTrigger1]
SystemTimingSlot = 4
```

```
PXI_STAR0 = 1
PXI_STAR1 = 2
PXI_STAR2 = 3
PXI_STAR3 = 5
PXI_STAR4 = 6
PXI_STAR5 = 7
PXI_STAR6 = 8

[Chassis1Slot1]
Model = “Example PXI Express System Model”
Vendor = “Example PXI Express System Vendor”
SlotType = PXIeSystemSlot2Link
SystemSlotLinkWidth1 = 4
SystemSlotLinkWidth2 = 4
SystemSlotLinkWidth3 = 4
SystemSlotLinkWidth4 = 4
ControllerModuleLinkWidth1 = 1
ControllerModuleLinkWidth2 = 1
ControllerModuleLinkWidth3 = 1
ControllerModuleLinkWidth4 = 1

[Chassis1Slot2]
Model = "Example PXI Express Peripheral Model"
Vendor = "Example PXI Express Peripheral Vendor"
ModelInstance = 1
PCIBusNumber = 2
PCIDeviceNumber = 15
SlotType = PXIeHybridSlot
SystemSlotLinkOrigin1 = 1
SystemSlotLinkOrigin2 = 4
PeripheralSlotLinkWidth1 = 4
PeripheralSlotLinkWidth2 = 0
PeripheralModuleLinkWidthMax = 1
PeripheralModuleLinkWidthNegotiated = 1

[Chassis1Slot3]
Model = "Example PXI Express Peripheral Model"
Vendor = "Example PXI Express Peripheral Vendor"
ModelInstance = 2
PCIBusNumber = 3
PCIDeviceNumber = 15
SlotType = PXIeHybridSlot
SystemSlotLinkOrigin1 = 2
SystemSlotLinkOrigin2 = 4
PeripheralSlotLinkWidth1 = 4
PeripheralSlotLinkWidth2 = 0
PeripheralModuleLinkWidthMax = 1
PeripheralModuleLinkWidthNegotiated = 1

[Chassis1Slot4]
Model = "Example PXI Express System Timing Model"
Vendor = "Example PXI Express System Timing Vendor"
ModelInstance = 1
PCIBusNumber = 4
```

```
PCIDeviceNumber = 15
LocalBusLeft = None
LocalBusRight = Chassis1Slot5
SlotType = PXIeSystemTimingSlot
SystemSlotLinkOrigin1 = 3
SystemSlotLinkOrigin2 = 4
PeripheralSlotLinkWidth1 = 4
PeripheralSlotLinkWidth2 = 0
PeripheralModuleLinkWidthMax = 4
PeripheralModuleLinkWidthNegotiated = 1

[Chassis1Slot5]
Model = "Example PXI-1 Model"
Vendor = "Example PXI-1 Vendor"
ModelInstance = 1
PCIBusNumber = 5
PCIDeviceNumber = 15
LocalBusLeft = Chassis1Slot4
LocalBusRight = Chassis1Slot6
SlotType = PXI-1Slot
SystemSlotLinkOrigin1 = 0
SystemSlotLinkOrigin2 = 4

[Chassis1Slot6]
Model = "Example PXI-1 Model"
Vendor = "Example PXI-1 Vendor"
ModelInstance = 2
PCIBusNumber = 5
PCIDeviceNumber = 14
LocalBusLeft = Chassis1Slot5
LocalBusRight = Chassis1Slot7
SlotType = PXI-1Slot
SystemSlotLinkOrigin1 = 0
SystemSlotLinkOrigin2 = 4

[Chassis1Slot7]
Model = "Example PXI-1 Model"
Vendor = "Example PXI-1 Vendor"
ModelInstance = 1
PCIBusNumber = 5
PCIDeviceNumber = 13
LocalBusLeft = Chassis1Slot6
LocalBusRight = Chassis1Slot8
SlotType = PXI-1Slot
SystemSlotLinkOrigin1 = 0
SystemSlotLinkOrigin2 = 4

[Chassis1Slot8]
Model = "Example PXI-1 Model"
Vendor = "Example PXI-1 Vendor"
ModelInstance = 1
PCIBusNumber = 5
PCIDeviceNumber = 12
LocalBusLeft = Chassis1Slot7
```

```
LocalBusRight = None
SlotType = PXI-1Slot
SystemSlotLinkOrigin1 = 0
SystemSlotLinkOrigin2 = 4
```

2.2 Chassis Description Files

Chassis description files characterize PXI Express Chassis. The primary purpose of a Chassis description file is to enumerate PXI trigger buses, system timing sets, sets of star triggers, and slots. Chassis description files are a key component in the PXI Express hardware description architecture, enabling a Resource Manager to generate a PXI Express system description.

RULE: A Chassis manufacturer SHALL provide a Chassis description file for each Chassis model produced.

RULE: A Chassis description file SHALL be named `chassis_`*`vendorDefinedText`*`.ini`, where *`vendorDefinedText`* is a vendor-defined string used to uniquely name a Chassis description file.

PERMISSION: A system controller module MAY place Chassis description files in any location, provided that the ChassisDescriptionFilePath registry value correctly points to this location. Refer to Section 4, *Software Frameworks and Requirements*, for the specific registry locator for a given operating system.

OBSERVATION: Using the ChassisDescriptionFilePath registry value, Chassis description file installers can copy their Chassis description files to a standard location. In addition, a PXI Express Resource Manager can use this location to identify the types of Chassis available for a PXI Express system.

2.2.1 Chassis Description Definitions

To develop a Chassis description, it is useful to define descriptors for the following Chassis components:

Chassis—A Chassis descriptor corresponds to a physical PXI Express Chassis. Chassis can include PCI bus segments, trigger buses, system timing sets, star triggers, and slots.

Trigger Bus—A PXI trigger bus descriptor corresponds to a physical trigger bus in a PXI Express Chassis. A trigger bus is characterized by a list of slots sharing the physical trigger bus connection. Chassis can contain multiple trigger buses.

Star Triggers—A PXI star trigger descriptor corresponds to a physical set of star triggers in a PXI Express Chassis. A set of star triggers is characterized by a star trigger controller slot number and a mapping of PXI_STAR lines to peripheral slot numbers. A Chassis can contain multiple sets of star triggers.

System Timing Sets—A System Timing Set descriptor corresponds to the set of system timing sets contained in a PXI Express Chassis. The system timing sets for a Chassis are characterized by the system timing slot number and a mapping of system timing sets to peripheral slot numbers. A Chassis can contain multiple system timing sets.

Slots–A PXI Express slot descriptor corresponds to a physical slot in a Chassis. A slot is characterized by a geographic address, a PCI logical address, local bus routings, and other special capabilities. A Chassis has multiple slots.

PXI-1 Bus Segment—A PXI-1 bus segment descriptor corresponds to physical PCI bus in a Chassis. PCI bus segments can contain slots, bridges, and other backplane devices. Multiple PCI bus segments are linked within a Chassis using PCI-PCI bridging.

2.2.2 Chassis Descriptor

A Chassis descriptor provides a high-level description of a PXI Express Chassis. A Chassis descriptor contains collections of the components that comprise a Chassis, including PCI bus segments, trigger buses, sets of star triggers, and slots.

RULE: A Chassis description file SHALL contain one and only one Chassis descriptor.

RULE: The Chassis descriptor section SHALL be named "Chassis."

RULE: Each Chassis descriptor section SHALL contain one of each tag line type described in Table 2-10.

Table 2-10. Chassis Description File—Chassis Tag Line Descriptions

Tag	Valid Values	Description
Model	A string indicating the model of this Chassis.	This tag identifies the Chassis model name.
Vendor	A string indicating the vendor of this Chassis.	This tag identifies the Chassis vendor name.
TriggerBusList	A comma-separated list of *n*, where *n* is a decimal integer such that *n* >= 1.	This tag enumerates the trigger buses in a Chassis.
StarSystemTimingSetList	A comma-separated list of *n*, where *n* is a decimal integer such that *n* >= 1.	This tag enumerates the PXI Express system timing sets in a Chassis.
StarTriggerList	A comma-separated list of *n*, where *n* is a decimal integer such that *n* >= 1.	This tag enumerates the sets of star trigger in a Chassis.
SlotList	A comma-separated list of *n*, where *n* is a decimal integer such that *n* >= 1.	This tag enumerates the slots in a Chassis.
PXI1BusSegmentList	A comma-separated list of n, where *n* is a decimal integer such that 1 <= *n* <= 255.	This tag enumerates the PXI-1 bus segments in a Chassis.

Chassis Descriptor Example

```
# This example describe an 8-slot PXI Express chassis with three hybrid
# peripheral slots (slots 2-4) and four PXI-1 slots (slots 5-8)
[Chassis]
Model = "Example 8-Slot Chassis"
Vendor = "PXISA"
TriggerBusList = 1
StarSystemTimingSetList = 1
StarTriggerList = 1
SlotList = 1,2,3,4,5,6,7,8
PXI1BusSegmentList = 1
```

RULE: Multiple PCI bus segments SHALL be uniquely numbered in the PXI1BusSegmentList tag.

OBSERVATION: PXI-1 bus segments can be numbered in an arbitrary fashion. For example, bus segments can be numbered according to their order of discovery using a depth-first PCI traversal algorithm.

RULE: Multiple trigger buses SHALL be uniquely numbered in the TriggerBusList tag.

OBSERVATION: Trigger buses can be numbered in an arbitrary fashion. For example, a trigger bus can be sequentially numbered based on the relative order of the slots it contains.

RULE: Multiple system timing sets SHALL be uniquely numbered in the StarSystemTimingSetList tag.

RULE: Multiple sets of star triggers SHALL be uniquely numbered in the StarTriggerList tag.

OBSERVATION: Sets of star triggers can be numbered in an arbitrary fashion. For example, a set of star triggers can be sequentially numbered based on the relative order of the slots the set contains.

RULE: PXI slots SHALL be uniquely numbered according to their corresponding physically viewable slot numbers.

2.2.3 Trigger Bus Descriptor

A trigger bus descriptor describes an individual trigger bus in a PXI Express Chassis. A trigger bus is characterized by a list of slots that reside on the trigger bus.

RULE: A Chassis description file SHALL contain a distinct PXI trigger bus descriptor for each physical PXI trigger bus in the Chassis.

RULE: A trigger bus descriptor SHALL be named "TriggerBus*N*," where *N* is the trigger bus number.

RULE: Trigger bus numbers SHALL be derived from the TriggerBusList tag of the Chassis descriptor (see Table 2-10).

OBSERVATION: While each trigger bus number will uniquely correspond to a set of PXI slots, there is not necessarily a one-to-one correspondence between trigger buses and PCI bus segments.

RULE: Each trigger bus descriptor SHALL contain one of each of the tag line types described in Table 2-11.

Table 2-11. Chassis Description File—Trigger Bus Tag Line Descriptions

Tag	Valid Values	Description
SlotList	A comma-separated list of *n*, where *n* is a decimal integer such that *n* >= 1.	This tag enumerates the slots on a trigger bus.

Trigger Bus Descriptor Example

```
# This example describe an 8-slot PXI Express chassis with three hybrid
# peripheral slots (slots 2-4) and four PXI-1 slots (slots 5-8).
# There is one trigger bus for this chassis spanning each of the 8 slots.
[TriggerBus1]
SlotList = 1,2,3,4,5,6,7,8
```

2.2.4 Star System Timing Sets Descriptor

A star system timing sets descriptor describes the system timing sets in a PXI Express Chassis. A star system timing sets descriptor is characterized by a system timing slot number and a mapping of system timing sets (that is, PXIe_DSTARA*n*, PXIe_DSTARB*n*, and PXIe_DSTARC*n*) to peripheral slot numbers.

RULE: A Chassis description file SHALL contain a distinct star system timing sets descriptor for each system timing slot in the Chassis.

RULE: A star system timing sets descriptor SHALL be named "StarSystemTimingSets*N*," where *N* is the number for the system timing sets.

RULE: Star system timing sets descriptors SHALL be derived from the StarSystemTimingSetsList tag of the Chassis descriptor (see Table 2-10).

RULE: Each star system timing sets descriptors SHALL contain one of each of the tab line types described in Table 2-12.

Table 2-12. Chassis Description File—Star System Timing Sets Tag Line Descriptions

Tag	Valid Values	Description
SystemTimingSlot	A decimal integer *n*, where *n* is a decimal integer such that *n* >= 1.	This tag specifies the slot number of the system timing slot for this group of system timing sets.
SystemTimingSet*n* (where *n* is a decimal integer such that 0 <= *n* <= 16), for each possible system timing set for a given system timing module.	A comma-separated list of *m*, where *m* is a decimal integer, corresponding to a PXI slot number, such that *m* >= 1.	This tag specifies the peripheral slot number corresponding to a set of PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC lines.

Star System Timing Sets Descriptor Example

```
# This example describe an 8-slot PXI Express chassis with three hybrid
# peripheral slots (slots 2-4) and four PXI-1 slots (slots 5-8).
# The system timing set controller slot is slot 2, and the system timing
# set mapping to each hybrid peripheral slot is described.
[StarSystemTimingSet1]
SystemTimingSlot = 2
SystemTimingSet0 = 2
SystemTimingSet1 = 3
SystemTimingSet2 = 4
```

2.2.5 Star Trigger Descriptor

A star trigger descriptor describes an individual set of star triggers in a PXI Express Chassis. A star trigger descriptor is characterized by a star trigger controller slot number and a mapping of PXI_STAR lines, as defined in the *PXI Hardware Specification*, to peripheral slot numbers.

RULE: A Chassis description file SHALL contain a distinct PXI star trigger descriptor for each physical set of star triggers in the Chassis.

RULE: A star trigger descriptor SHALL be named "StarTrigger*N*," where *N* is the number for the set of star triggers.

RULE: Star trigger descriptor numbers SHALL be derived from the StarTriggerList tag of the Chassis descriptor (see Table 2-10).

RULE: Each star trigger descriptor SHALL contain one of each of the tag line types described in Table 2-13.

Table 2-13. Chassis Description File—Star Trigger Tag Line Descriptions

Tag	Valid Values	Description
SystemTimingSlot	A decimal integer *n*, where *n* is a decimal integer such that *n* >= 1.	This tag specifies the star trigger controller slot number for a set of star triggers.
PXI_STAR*n* (where *n* is a decimal integer such that 0 <= *n* <= 16), for each PXI star trigger line routed to a PXI slot.	A comma-separated list of *m*, where *m* is a decimal integer, corresponding to a PXI slot number, such that *m* >= 1.	This tag specifies the PXI_STAR line to slot number mapping for a set of star triggers.

Star Trigger Descriptor Example

```
# This example describe an 8-slot PXI Express chassis with three hybrid
# peripheral slots (slots 2-4) and four PXI-1 slots (slots 5-8).
# The star trigger controller slot is slot 2, and the PXI_STAR lines
# connect to each of the chassis' peripheral slots (2-8).
[StarTrigger1]
ControllerSlot = 2
PXI_STAR0 = 3
PXI_STAR1 = 4
PXI_STAR2 = 5
PXI_STAR3 = 6
PXI_STAR4 = 7
PXI_STAR5 = 8
```

2.2.6 PXI-1 Bus Segment Descriptor

A PXI-1 bus segment descriptor characterizes a PCI bus segment containing PXI-1 slots or hybrid slots in a PXI Express Chassis. The most important aspect of a PCI bus segment descriptor is that it describes the mapping from PCI address lines (AD[31:0]) to IDSEL assignments for the segment's slots.

RULE: A Chassis description file SHALL contain a distinct PXI-1 bus segment descriptor for each physical PCI bus segment containing PXI-1 or hybrid slots in a Chassis.

RULE: A PXI-1 bus segment descriptor SHALL be named "PXI1BusSegment*N*," where *N* is the PXI-1 bus segment number.

RULE: PXI-1 bus segment numbers SHALL be derived from the PXI1BusSegmentBusList tag of the Chassis descriptor (see Table 2-10).

OBSERVATION: While each PXI-1 bus segment number will uniquely correspond to a PCI bus number, the PCI bus segment number will not necessarily be equal to the corresponding PCI bus number.

RULE: Each PXI-1 bus segment descriptor SHALL contain one of each of the tag line types described in Table 2-14.

Table 2-14. Chassis Description File—PXI-1 Bus Segment Tag Line Descriptions

Tag	Valid Values	Description
SlotList	A comma-separated list of *n*, where *n* is a decimal integer such that *n* >= 1.	This tag enumerates the slots on a PCI bus segment.
IDSELList	*n*, where *n* is a decimal integer such that 1 <= *n* <= 31.	This tag lists the PCI address line numbers (AD[31:0]) used to implement the IDSEL signals for devices on a PCI bus segment.
IDSEL*n,* where *n* is a decimal integer corresponding to a PCI address line (AD[31:0]), for each *n* contained in the IDSELList	A slot descriptor. (Other.)	This tag specifies the PCI address line number (AD[31:0]) used to implement the IDSEL signal for a given slot, bridge, or backplane device on a PCI bus segment.

PXI-1 Bus Segment Descriptor Example

```
# This example describe an 8-slot PXI Express chassis with three hybrid
# peripheral slots (slots 2-4) and four PXI-1 slots (slots 5-8).
[PXI1BusSegment1]
SlotList = 5,6,7,8
IDSELList = 31,30,29,28
IDSEL31 = Slot5
IDSEL30 = Slot6
IDSEL29 = Slot7
IDSEL28 = Slot8
```

RULE: Slots SHALL be uniquely numbered in the SlotList tag.

OBSERVATION: Slot numbers will correspond to physically-viewable slot numbers for a PCI bus segment. In addition, the SlotList will be a subset of the SlotList specified in the Chassis descriptor (see Table 2-10).

PERMISSION: A PCI bus segment descriptor MAY specify an IDSEL routing to a backplane device other than a slot or a bridge.

2.2.7 Slot Descriptor

A slot descriptor describes an individual slot in a PXI Express Chassis. A slot descriptor is characterized by the features of the slot it describes.

RULE: A Chassis description file SHALL contain a distinct slot descriptor for each physical slot in the Chassis.

RULE: A slot descriptor SHALL be named "Slot*N*," where *N* is the physical slot number.

RULE: A slot number SHALL be derived by enumerating IDSEL assignments for the corresponding PXI-1 bus segment descriptor (see Table 2-14).

PERMISSION: A slot number MAY be derived from alternate sources, including a Chassis descriptor's SlotList tag (see Table 2-10).

RULE: Each slot descriptor that describes a PXI-1 or hybrid slot SHALL contain one of each of the nonshaded tag line types described in Table 2-15.

OBSERVATION: A PXI Express slot does not need to implement any of the fields in Table 2-15, because these slots do not implement the PXI-1 fields described in the table. These slot descriptors will not contain any tags.

Table 2-15. Chassis Description File—Slot Tag Line Descriptions

Tag	Valid Values	Description
LocalBusLeft	A valid slot descriptor. A valid star trigger descriptor. (Other.)	This tag indicates how this slot routes its local bus pins to the left.
LocalBusRight	A valid slot descriptor. (Other.)	This tag indicates how this slot routes its local bus pins to the right.

Slot Descriptor Examples

PXI-1 Slot Example

```
# This example describe an 8-slot PXI Express chassis with three hybrid
# peripheral slots (slots 2-4) and four PXI-1 slots (slots 5-8).
# The slot described is a PXI-1 slot.

[Slot7]
LocalBusLeft = Slot6
LocalBusRight = Slot8
```

Hybrid Peripheral Slot Example

```
# This example describe an 8-slot PXI Express chassis with three hybrid
# peripheral slots (slots 2-4) and four PXI-1 slots (slots 5-8).
# The slot described is a hybrid peripheral slot.

[Slot4]
# Note that no LocalBus tags apply because this is not a PXI-1 slot.
```

2.2.8 Chassis Description File Examples

The following are complete examples of Chassis description files.

```
# This example describe an 8-slot PXI Express chassis with three hybrid
# peripheral slots (slots 2-4) and four PXI-1 slots (slots 5-8)
[Chassis]
Model = "Example 8-Slot Chassis"
Vendor = "PXISA"
TriggerBusList = 1
StarSystemTimingSetList = 1
StarTriggerList = 1
SlotList = 1,2,3,4,5,6,7,8
PXI1BusSegmentList = 1

# There is one trigger bus for this chassis spanning each of the 8 slots.
[TriggerBus1]
```

```
SlotList = 1,2,3,4,5,6,7,8

# The system timing set controller slot is slot 2, and the system timing set
# mapping to each hybrid peripheral slot is described.
[StarSystemTimingSet1]
ControllerSlot = 2
SystemTimingSet0 = 2
SystemTimingSet1 = 3
SystemTimingSet2 = 4

# The star trigger controller slot is slot 2, and the PXI_STAR lines connect
# to each of the chassis' peripheral slots (2-8).
[StarTrigger1]
ControllerSlot = 2
PXI_STAR0 = 3
PXI_STAR1 = 4
PXI_STAR2 = 5
PXI_STAR3 = 6
PXI_STAR4 = 7
PXI_STAR5 = 8

[PXI-1BusSegment1]
SlotList = 5,6,7,8
IDSELList = 31,30,29,28
IDSEL31 = Slot5
IDSEL30 = Slot6
IDSEL29 = Slot7
IDSEL28 = Slot8

[Slot2]
# Note that no LocalBus tags apply because this is not a PXI-1 slot.

[Slot3]
# Note that no LocalBus tags apply because this is not a PXI-1 slot.

[Slot4]
# Note that no LocalBus tags apply because this is not a PXI-1 slot.

[Slot5]
LocalBusLeft = None
LocalBusRight = Slot6

[Slot6]
LocalBusLeft = Slot5
LocalBusRight = Slot7

[Slot7]
LocalBusLeft = Slot6
LocalBusRight = Slot8

[Slot8]
LocalBusLeft = Slot7
LocalBusRight = None
```

3. PXI Express Software Services

This section defines the PXI Express Software Services, their APIs, their registration, and how they interact with the PXI Express Resource Manager.

3.1 Overview

This section defines the services that shall be implemented for each component of the PXI Express system. It further defines how those services should be registered and how they are used by the PXI Express Resource Manager in the system.

The APIs and databases defined in this section are described in a platform-independent manner. The platform-specific details of this specification are found in Section 4, *Software Frameworks and Requirements*.

3.2 PXI Express Components

Certain PXI Express components are enumerated by the PXI Express Resource Manager by interacting with software included with those components. These components include:

- System Modules
- Peripheral Modules
- Chassis

These components must include software to allow the PXI Express Resource Manager and other clients to gather information about the module and use its standard features. As such, this specification imposes requirements on the software that ships with those modules. This software is referred to as a driver. The driver need not be a driver as defined by the operating system involved. For the purpose of this specification, the driver for a component is that software included with the component that implements the interfaces in this specification.

3.3 Service Types

The drivers in a PXI Express system must support the operations listed in this section. The operations are specified here by their names, input parameters, and output parameters. Output parameters are differentiated by an asterisk in the parameter list. Although this corresponds roughly to the C language notation for passing a pointer, it does not necessarily indicate that a pointer is used in the implementation.

Consult the appropriate software framework section in Section 4, *Software Frameworks and Requirements*, for calling conventions and type definitions for these operations.

3.3.1 System Module Drivers

A PXI Express System Module driver is responsible for:

- Enumerating its System Modules.
- Providing information about the attributes of each System Module.
- Providing bus enumeration information about each System Module.
- Providing access to the Chassis EPROMs.
- Providing access to the SMBus.

RULE: A System Module driver SHALL contain the following operations.

```
Status PXISA_SystemModule_GetCount(String vendor, String model, Integer * count)
```
vendor: Vendor name to match.
model: Model name to match.
count: Number of System Modules found by the driver.

RULE: If a System Module driver maintains a cache of System Module names, the System Module driver SHALL update that cache when `PXI_SMGetCount` is invoked.

```
Status PXISA_SystemModule_GetName(String vendor, String model, Integer index,
String * name, String * addressInfo)
```
vendor: Vendor name to match.
model: Model name to match.
index: Index of a System Module.
name: Unique name of a System Module.
addressInfo: Additional addressing information for the module.

```
Status PXISA_SystemModule_GetInformation(String name, String addressInfo, Integer
field, Integer * value);
```
name: Unique name of a System Module.
addressInfo: Additional addressing information for the System Module.
field: Selector for which information field is requested.
value: Value of the information field.

Field	Value
0	Maximum Link 1 Width in 2 Link Mode
1	Maximum Link 2 Width in 2 Link Mode
2	Maximum Link 1 Width in 4 Link Mode
3	Maximum Link 2 Width in 4 Link Mode
4	Maximum Link 3 Width in 4 Link Mode
5	Maximum Link 4 Width in 4 Link Mode
100	Number of valid links
101	PCI Bus Number of Link 1
102	PCI Bus Number of Link 2
103	PCI Bus Number of Link 3 (valid for 4 link mode)
104	PCI Bus Number of Link 4 (valid for 4 link mode)
105	Subordinate PCI Bus Number for parent bridge of the bus of Link 1
106	Subordinate PCI Bus Number for parent bridge of the bus of Link 2
107	Subordinate PCI Bus Number for parent bridge of the bus of Link 3
108	Subordinate PCI Bus Number for parent bridge of the bus of Link 4

```
Status PXISA_SystemModule_GetChassisEeprom(String name, String addressInfo,
Buffer * chassisEeprom);
```

name: Unique name of a System Module.
addressInfo: Additional addressing information for the System Module.
chassisEeprom: Contents of the Chassis EEPROM. This buffer must be 256 bytes.

```
Status PXISA_SystemModule_SMBusOperation(String name, String addressInfo, Integer
protocol, Integer address, Integer command, Integer packetErrorCode, Integer
writeBufferCount, Buffer writeBuffer, Integer * readBufferCount, Buffer *
readBuffer);
```

name: Unique name of a System Module.
addressInfo: Additional addressing information for the System Module.
protocol: Protocol used for the SMBus operation.

Protocol	Value	Notes
Quick Command	0	The command, pec, and buffer parameters are ignored. Only the address is sent.
Send Byte	1	The command parameter is ignored. The first byte of the writeMessage parameter is sent.
Receive Byte	2	The command parameter is ignored. The received byte is placed into the first byte of the readMessage parameter.
Write Byte	3	
Read Byte	4	
Write Word	5	
Read Word	6	
Process Call	7	
Write Block	8	
Read Block	9	

address: Address Byte sent to the device.

command: Command byte to send to the device.

packetErrorCode: Flag to specify whether to include the Packet Error Code. The value of this field should be zero (0) when the PEC should not be included, and one (1) when the PEC should be included.

writeBufferCount: Number of bytes to be written for Write Block commands.

writeBuffer: Data content of the operation.

readBufferCount: Number of bytes received for Read Block commands.

readBuffer: Data content received by the operation. This buffer must be 32 bytes.

3.3.2 Chassis Drivers

A PXI Express Chassis driver is responsible for providing bus enumeration information about each Chassis. Specifically, the Chassis driver provides the bus numbers of PCI buses used in PXI-1 slots and hybrid slots. Most Chassis information is discovered not through the Chassis driver, but through the System Module driver via the EPROM. Chassis topology information is maintained in the PXI Express Chassis description file.

The operations described here return information about PXI-1 and legacy buses in a Chassis directly connected to a PCI Express to PCI bridge. These root buses are enumerated in the Chassis Description file. These buses can be characterized by the Chassis vendor name, the Chassis model name, the index of the root bus in the Chassis (as numbered in the Chassis Description file), and an instance number (for systems with multiple Chassis).

```
Status PXISA_Chassis_GetCount(String vendor, String model, Integer * count)
```
vendor: Vendor name to match.
model: Model name to match.
count: Number of chassis found by the driver, matching the criteria of the other parameters.

RULE: If a Chassis driver maintains a cache of PCI root buses, the Chassis driver SHALL update that cache when `PXISA_Chassis_GetCount` is invoked.

```
Status PXISA_Chassis_GetPCIRootBusNumber(String vendor, String model, Integer
rootIndex, Integer chassisIndex, Integer * busNumber)
```
vendor: Vendor name of the Chassis.
model: Model name of the Chassis.
rootIndex: Index of the bus as given in the Chassis description file.
chassisIndex: Instance number to differentiate this bus from those found in other Chassis.
busNumber: PCI bus number of the selected bus.

OBSERVATION: A client of a chassis driver cannot assume that root PCI bus numbers corresponding to the same chassis index are necessarily in the same chassis. The client must correlate the reported bus numbers with the bus number information reported by the system module drivers in order to determine which bus numbers reside in which chassis. See Section 3.5, system enumeration, for more information.

3.3.3 Peripheral Module Drivers

A PXI Express Peripheral module driver is responsible for:

- Enumerating its Peripheral Modules.
- Providing the geographical address of each Peripheral Module.
- Reporting bus enumeration information about each Peripheral Module.

```
Status PXISA_PeripheralModule_GetCount(String vendor, String model, Integer *
count)
```
vendor: Vendor name to match.
model: Model name to match.
pmCount: Number of Peripheral Modules found by the driver, matching the criteria of the other parameters.

RULE: If a Peripheral Module driver maintains a cache of Peripheral Module names, the Chassis driver SHALL update that cache when PXISA_PeripheralModule_GetCount is invoked.

```
Status PXISA_PeripheralModule_GetName(String vendor, String model, Integer index,
String * name, String * addressInfo)
```
vendor: Vendor name to match.
model: Model name to match.
index: Index of a Peripheral Module.

name: Unique name of a Peripheral Module.
addressInfo: Additional addressing information for the module.

```
Status PXISA_PeripheralModule_GetInformation(String name, String addressInfo,
Integer field, Integer * value);
```

name: Unique name of a Peripheral Module.
addressInfo: Additional addressing information for the Peripheral Module.
field: Selector for which information field is requested.
value: Value of the information field.

Field	Value
0	Maximum Link Width
100	PCI Bus Number
101	Negotiated Link Width
102	Slot Number

3.3.4 Status Codes

All of the operations defined for PXI Express System Module, Chassis, and Peripheral Module drivers return a status code.

RULE: A status code of zero (0) SHALL be used to represent a successful operation.

RULE: A negative status code SHALL be used to represent a failure. The status code negative one (–1) is reserved by this specification to represent a generic failure.

OBSERVATION: A driver may return other values to indicate a specific type of failure, as long as those values are less than negative one.

RULE: A positive status code SHALL be used to represent a warning. The status code one (1) is reserved by this specificaiton to represent a generic warning.

OBSERVATION: A driver may return other values to indicate a specific type of warning, as long as those values are greater than one.

3.4 Registration of Services

The drivers implementing the PXI Express Services will be invoked by clients. Sometimes, the drivers will be invoked to discover system components. At other times, the drivers will be invoked to perform operations on components that have already been discovered. In either case, the clients need a central registry where they can find information about how to invoke the driver. This central registry is called the *Services Tree*.

RULE: Drivers SHALL include an installer that places references to the driver in the Services Tree, as described in this section.

3.4.1 Services Tree

The Services Tree is a hierarchical database of the services available in a PXI Express system. Each element in the Services Tree is either a *key* or an *attribute*.

Each key has:

- One name.
- One parent key (exception, the root key has no parent).
- Zero or more child keys.
- Zero or more attributes.

Each attribute has:

- One name.
- One type, which is either Integer or String.
- One value.

A key's *descendant keys* are that key's child keys, and the child keys' descendants.

The root of the Services Tree is named "Services."

The child keys of the root are called *category keys*. The names of the category keys are "System Modules," "Chassis," and "Peripheral Modules."

The child keys of the category keys are called *vendor keys*. The manufacturer keys and their descendants are created by the installation software for the PXI Express drivers. The name of a vendor key is a unique string identifying the vendor of the component managed by the driver being installed.

PERMISSION: A vendor key MAY have an optional attribute named "VendorName," whose type is string and whose value is another form of the vendor name.

RULE: The "VendorName" attribute described in the permission above SHALL NOT be used for any purpose except to provide more readable vendor name.

The child keys of the vendor keys are called *model keys*. The name of a model key is the model name of the component being installed. This name SHALL be unique for the vendor of that model.

RULE: Each vendor key SHALL have an attribute whose name is "Library" and whose value is the path to the library implementing the driver for that system component.

RULE: Each vendor key SHALL have an integer attribute whose name is "Version" and whose value is 0x00010000.

3.5 System Enumeration

A *Resource Manager* is defined as the entity responsible for creating the PXI system description file and PXI Express system description file. For example, the responsibilities of a Resource Manager might be accomplished by a systems integrator, or a software utility might be provided to automate the Resource Manager algorithm.

RULE: A system controller module manufacturer SHALL provide either a system description file for each supported system configuration or a Resource Manager utility that can manage the system description file.

RECOMMENDATION: A system controller module manufacturer SHOULD provide a utility that can automate the Resource Manager algorithm.

The PXI Express Resource Manager gathers information about the system using the Services Tree, the component drivers, and the description files specified in this specification and in the *PXI Software Specification*. The PXI Express Resource Manager reports this information in two files:

- A PXI Express system description file as defined in this specification, describing the PXI Express features of the system.
- A PXI system description file as defined in the *PXI Software Specification*, describing the features of the system compatible with PXI-1.

3.5.1 Resource Manager Algorithm

RULE: The Resource Manager SHALL execute the following algorithm:

1. For each model key in the "System Module" category key, the Resource Manager loads the installed library for that vendor and model and enumerates the System Modules.
2. For each System Module found, the Resource Manager reads the names, attributes, and Chassis EPROM.
3. For each model key in the "Peripheral Module" category key, the Resource Manager loads the installed library for that vendor and model and enumerates the peripherals.
4. For each Peripheral Module found, the Resource Manager reads the names and attributes.
5. The Resource Manager matches the System Module PCI bus numbers and PCI subordinate bus numbers to the bus numbers reported by the Peripheral Module drivers, recording which Peripheral Module is in which Chassis. (See Section 3.5.2.)
6. The Resource Manager matches the System Module PCI bus numbers and PCI subordinate bus numbers to PCI root buses reported by the Chassis drivers.
7. The Resource Manager traverses the PCI root buses, finds subordinate bridges, and determines the bus numbers and device numbers for each slot connected to a PCI bus (either a hybrid or PXI-1 slot).
8. The Resource Manager traverses the PCI root buses of PXI-1 Chassis, finds subordinate bridges, and determines the bus numbers and device numbers for each slot.
9. The Resource Manager writes all the information to the PXI Express and PXI system description files (`pxiesys.ini`, `pxisys.ini`).

RULE: The Resource Manager SHALL load all libraries and keep them loaded until it has performed all operations on those libraries for a run of the Resource Manager Algorithm.

OBSERVATION: The preceding rule is intended to improve performance when the same library is used for multiple components. Deferring the unloading of the library allows an implementation to increment a reference count instead of reloading the library repeatedly.

PERMISSION: A Resource Manager MAY execute a variation of the specified algorithm if the results and side effects would be the same as for an implementation of the specified algorithm.

3.5.2 Determining Chassis Numbers

In the Resource Manager algorithm above, one of the responsibilities of the Resource Manager is to determine in which Chassis a Peripheral Module is located. This is accomplished by examining the bus numbers and subordinate bus numbers of the System Modules and the bus numbers and Peripheral Modules.

According to the specifications for PCI Express, each link on the System Module connected to the Chassis will have a virtual PCI-PCI bridge associated with that link. That PCI-PCI bridge will have a bus number for the link, and a subordinate bus number indicating the most deeply nested bus number that is subordinate to that bridge. By comparing peripheral bus numbers to the bus numbers and subordinate bus numbers of the system controller, a Resource Manager can determine whether a peripheral device is a downstream of a system controller.

In a system with multiple Chassis, a system integrator may connect a Chassis to another Chassis via a cabling solution that preserves PCI semantics. In this case, there may be multiple system controllers upstream from the System Module. To handle this case, the resource manager must choose the system controller whose link is the closest to the Peripheral Module. This choice will be made by selecting the system controller link upstream from the Peripheral Module with the highest bus number.

RULE: A Resource Manager SHALL provide the ability to assign arbitrary Chassis numbers.

3.5.3 Handling Driver Errors

RULE: A PXI Express Resource Manager SHALL use the status codes returned from the driver as follows:

1. If a driver returns an error code, the Resource Manager SHALL stop execution and report an error to the user.
2. If a driver returns a warning, the Resource Manager SHALL proceed as if the driver returned success.

RECOMMENDATION: A PXI Express Resource Manager SHOULD issue a diagnostic when a driver returns a warning.

PERMISSION: A PXI Express Resource Manager MAY provide additional configuration options to allow for other methods of handling errors and warnings, such as ignoring specific errors, aborting in response to specific warnings, or disabling drivers that report errors.

4. Software Frameworks and Requirements

This section discusses the framework specific details of a PXI Express system. It gives an overview of the software requirements for components in a PXI Express system, along with framework-specific definitions and bindings for the software libraries described in previous sections of this specification.

4.1 Overview

The *PXI-2: PXI Software Specification* describes the software requirements for components in a PXI system and the supported frameworks for software in PXI. This specification builds on those definitions in PXI-2 by defining the binding and linkage protocols for drivers in each software framework.

4.2 PXI Software Compatibility

The *PXI-2: PXI Software Specification* describes the software requirements for components in a PXI system and the supported frameworks for software in PXI. This specification builds on those definitions in PXI-2 by defining the binding and linkage protocols for drivers in each software framework.

RULE: PXI Express System Modules, Peripheral Modules, and Chassis SHALL comply with *Chapter 3: Software Frameworks and Requirements* of the specification *PXI-2:PXI Software Specification*.

4.3 32-bit Windows System Framework

4.3.1 Introduction

In addition to the requirements in *PXI-2: PXI Software Specification*, this specification describes additional requirements for driver software for PXI components.

4.3.2 System Description File Location

RULE: PXI Express and PXI system description files SHALL be located in the `<windows>` directory (for example, `c:\windows` or `c:\winnt`).

4.3.3 Chassis Description File Path Location

RULE: A system controller module SHALL provide the following Windows registry value for specifying a location of Chassis description files:

Key: HKEY_LOCAL_MACHINE\SOFTWARE\PXISA\CurrentVersion

Value: ChassisDescriptionFilePath

The ChassisDescriptionFilePath SHALL be a string value that specifies the complete path of a directory that holds Chassis description files.

4.3.4 Driver Software Bindings

RULE: The drivers defined in this specification SHALL be implemented as Windows DLLs, with each operation corresponding to an exported symbol of the DLL.

A DLL implementing a driver defined by this specification is called a PXI driver DLL.

RULE: A PXI driver DLL SHALL export all symbols by name.

RULE: A PXI driver DLL SHALL use stdcall as the calling convention for all entry points.

RULE: A PXI driver DLL SHALL use the following C data types to represent the data types given in the function definitions.

Operation data type	Input parameter type	Output parameter type
Integer	long	long *
Status	long	N/A
String	const char*, pointing to a null terminated string	char*, pointing to a buffer of 256 characters
Buffer	const char*; pointing to a buffer of a length specified by the operation	char*, pointing to a buffer of a length specified by the operation

4.3.5 Services Tree Implementation

The Services Tree is implemented in the Windows registry, as described in this section.

RULE: The root of the services tree SHALL be located in the Windows registry at the following key:

HKEY_LOCAL_MACHINE\SOFTWARE\PXISA\Services

RULE: The name of a key in the Services Tree SHALL be the key name of that key in the Windows registry. An attribute SHALL be implemented as a value in the Windows registry. The types of the Service Tree key attributes SHALL be implemented using the following registry types.

Services Tree type	Windows Registry type
Integer	DWORD (REG_DWORD)
String	String (REG_SZ)

Appendix: 32-Bit Windows System Framework Files

PXIExpress.h

```
/*-----------------------------------------------------------------------------*/
/*                                                                             */
/* Title   : PXIExpress.h                                                      */
/* Date    : 07-06-2005                                                        */
/* Purpose : Definitions for using PXI Express System Module, Chassis, and     */
/*           Peripheral Module drivers, compliant with revision 1.0 of the     */
/*           PXI Express Software Specification.                               */
/*                                                                             */
/*-----------------------------------------------------------------------------*/

#if !defined (___pxiexpress_h___)
#define       ___pxiexpress_h___


/*-----------------------------------------------------------------------------*/
/*                                                                             */
/* Definitions common to PXI Express System Module, Chassis, and Peripheral    */
/* Module drivers.                                                             */
/*                                                                             */
/*-----------------------------------------------------------------------------*/

#define _PXISA_FUNC _stdcall

#define _PXISA_PTR *

typedef long                          tPXISA_Status;
typedef long                          tPXISA_Integer;
typedef long _PXISA_PTR               tPXISA_PInteger;
typedef char                          tPXISA_Char;
typedef tPXISA_Char const _PXISA_PTR tPXISA_StringConstant;
typedef tPXISA_Char _PXISA_PTR       tPXISA_String;
typedef tPXISA_Char const _PXISA_PTR tPXISA_BufferConstant;
typedef tPXISA_Char _PXISA_PTR       tPXISA_Buffer;

enum
{
   kPXISA_StringLength = 256
};

enum ePXISA_Status
{
   kPXISA_Success = 0,

   kPXISA_Error   = -1,

   kPXISA_Warning = 1
};
```

```
#define PXISA_Failed(Status) (kPXISA_Success > (Status))


/*---------------------------------------------------------------------------*/
/*                                                                           */
/* Definitions for PXI Express System Module drivers.                        */
/*                                                                           */
/*---------------------------------------------------------------------------*/

/* PXI Express System Module GetCount function */

#define kPXISA_SystemModule_GetCount_String "PXISA_SystemModule_GetCount"

typedef tPXISA_Status (_PXISA_FUNC _PXISA_PTR tPXISA_SystemModule_GetCount) (
   tPXISA_StringConstant vendor,
   tPXISA_StringConstant model,
   tPXISA_PInteger       count
   );

/* PXI Express System Module GetName function */

#define kPXISA_SystemModule_GetName_String "PXISA_SystemModule_GetName"

typedef tPXISA_Status (_PXISA_FUNC _PXISA_PTR tPXISA_SystemModule_GetName) (
   tPXISA_StringConstant vendor,
   tPXISA_StringConstant model,
   tPXISA_Integer        index,
   tPXISA_String         name,
   tPXISA_String         addressInfo
   );

/* PXI Express System Module GetInformation function */

#define kPXISA_SystemModule_GetInformation_String
"PXISA_SystemModule_GetInformation"

enum ePXISA_SystemModule_GetInformation_Field
{
   kPXISA_SystemModule_MaximumLink1WidthIn2LinkMode             = 0,
   kPXISA_SystemModule_MaximumLink2WidthIn2LinkMode             = 1,
   kPXISA_SystemModule_MaximumLink1WidthIn4LinkMode             = 2,
   kPXISA_SystemModule_MaximumLink2WidthIn4LinkMode             = 3,
   kPXISA_SystemModule_MaximumLink3WidthIn4LinkMode             = 4,
   kPXISA_SystemModule_MaximumLink4WidthIn4LinkMode             = 5,

   kPXISA_SystemModule_NumberOfValidLinks                       = 100,
   kPXISA_SystemModule_Link1BusNumber                           = 101,
   kPXISA_SystemModule_Link2BusNumber                           = 102,
   kPXISA_SystemModule_Link3BusNumber                           = 103,
   kPXISA_SystemModule_Link4BusNumber                           = 104,
   kPXISA_SystemModule_Link1BusParentBridgeSubordinateBusNumber = 105,
   kPXISA_SystemModule_Link2BusParentBridgeSubordinateBusNumber = 106,
   kPXISA_SystemModule_Link3BusParentBridgeSubordinateBusNumber = 107,
   kPXISA_SystemModule_Link4BusParentBridgeSubordinateBusNumber = 108
```

```
};

typedef tPXISA_Status (_PXISA_FUNC _PXISA_PTR tPXISA_SystemModule_GetInformation)
(
   tPXISA_StringConstant name,
   tPXISA_StringConstant addressInfo,
   tPXISA_Integer        field,
   tPXISA_PInteger       value
   );

/* PXI Express System Module GetChassisEEPROM function */

#define kPXISA_SystemModule_GetChassisEEPROM_String
"PXISA_SystemModule_GetChassisEEPROM"

enum
{
   kPXISA_ChassisEEPROM_BufferLength = 256
};

typedef tPXISA_Status (_PXISA_FUNC _PXISA_PTR
tPXISA_SystemModule_GetChassisEEPROM) (
   tPXISA_StringConstant name,
   tPXISA_StringConstant addressInfo,
   tPXISA_Buffer         chassisEeprom
   );

/* PXI Express System Module SMBusOperation function */

#define kPXISA_SystemModule_SMBusOperation_String
"PXISA_SystemModule_SMBusOperation"

enum ePXISA_SMBus_Protocol
{
   kPXISA_SMBus_QuickCommand     = 0,
   kPXISA_SMBus_SendByte         = 1,
   kPXISA_SMBus_ReceiveByte      = 2,
   kPXISA_SMBus_WriteByte        = 3,
   kPXISA_SMBus_ReadByte         = 4,
   kPXISA_SMBus_WriteWord        = 5,
   kPXISA_SMBus_ReadWord         = 6,
   kPXISA_SMBus_ProcessCall      = 7,
   kPXISA_SMBus_WriteBlock       = 8,
   kPXISA_SMBus_ReadBlock        = 9
};

enum
{
   kPXISA_SMBus_BlockBufferSize = 32
};

typedef tPXISA_Status (_PXISA_FUNC _PXISA_PTR tPXISA_SystemModule_SMBusOperation)
(
   tPXISA_StringConstant name,
```

```
   tPXISA_StringConstant addressInfo,
   tPXISA_Integer        protocol,
   tPXISA_Integer        address,
   tPXISA_Integer        command,
   tPXISA_Integer        packetErrorCode,
   tPXISA_Integer        writeBufferCount,
   tPXISA_BufferConstant writeBuffer,
   tPXISA_PInteger       readBufferCount,
   tPXISA_Buffer         readBuffer
   );


/*-----------------------------------------------------------------------------*/
/*                                                                             */
/* Definitions for PXI Express Chassis drivers.                                */
/*                                                                             */
/*-----------------------------------------------------------------------------*/

/* PXI Express Chassis GetCount function */

#define kPXISA_Chassis_GetCount_String "PXISA_Chassis_GetCount"

typedef tPXISA_Status (_PXISA_FUNC _PXISA_PTR tPXISA_Chassis_GetCount) (
   tPXISA_StringConstant vendor,
   tPXISA_StringConstant model,
   tPXISA_PInteger       count
   );

/* PXI Express Chassis GetPCIRootBusNumber function */

#define kPXISA_Chassis_GetPCIRootBusNumber_String
"PXISA_Chassis_GetPCIRootBusNumber"

typedef tPXISA_Status (_PXISA_FUNC _PXISA_PTR tPXISA_Chassis_GetPCIRootBusNumber)
(
   tPXISA_StringConstant vendor,
   tPXISA_StringConstant model,
   tPXISA_Integer        rootIndex,
   tPXISA_Integer        chassisIndex,
   tPXISA_PInteger       busNumber
   );


/*-----------------------------------------------------------------------------*/
/*                                                                             */
/* Definitions for PXI Express Peripheral Module drivers.                      */
/*                                                                             */
/*-----------------------------------------------------------------------------*/

/* PXI Express Peripheral Module GetCount function */

#define kPXISA_PeripheralModule_GetCount_String
"PXISA_PeripheralModule_GetCount"
```

```
typedef tPXISA_Status (_PXISA_FUNC _PXISA_PTR tPXISA_PeripheralModule_GetCount) (
   tPXISA_StringConstant vendor,
   tPXISA_StringConstant model,
   tPXISA_PInteger       count
   );

/* PXI Express Peripheral Module GetName function */

#define kPXISA_PeripheralModule_GetName_String "PXISA_PeripheralModule_GetName"

typedef tPXISA_Status (_PXISA_FUNC _PXISA_PTR tPXISA_PeripheralModule_GetName) (
   tPXISA_StringConstant vendor,
   tPXISA_StringConstant model,
   tPXISA_Integer        index,
   tPXISA_String         name,
   tPXISA_String         addressInfo
   );

/* PXI Express Peripheral Module GetInformation function */

#define kPXISA_PeripheralModule_GetInformation_String
"PXISA_PeripheralModule_GetInformation"

enum ePXISA_PeripheralModule_GetInformation_Field
{
   kPXISA_PeripheralModule_MaximumLinkWidth    = 0,

   kPXISA_PeripheralModule_BusNumber           = 100,
   kPXISA_PeripheralModule_NegotiatedLinkWidth = 101,
   kPXISA_PeripheralModule_SlotNumber          = 102
};

typedef tPXISA_Status (_PXISA_FUNC _PXISA_PTR
tPXISA_PeripheralModule_GetInformation) (
   tPXISA_StringConstant name,
   tPXISA_StringConstant addressInfo,
   tPXISA_Integer        field,
   tPXISA_PInteger       value
   );

#endif /* #if !defined (___pxiexpress_h___) */
```

PXIExpressSystemModule.def

```
; Module definition file for a PXI Express System Module driver.
EXPORTS
   PXISA_SystemModule_GetCount           @101
   PXISA_SystemModule_GetName            @102
   PXISA_SystemModule_GetInformation     @103
   PXISA_SystemModule_GetChassisEEPROM   @104
   PXISA_SystemModule_SMBusOperation     @105
```

PXIExpressChassis.def

```
; Module definition file for a PXI Express Chassis driver.
EXPORTS
   PXISA_Chassis_GetCount                @201
   PXISA_Chassis_GetPCIRootBusNumber     @202
```

PXIExpressPeripheralModule.def

```
; Module definition file for a PXI Express Peripheral Module driver.
EXPORTS
   PXISA_PeripheralModule_GetCount       @301
   PXISA_PeripheralModule_GetName        @302
   PXISA_PeripheralModule_GetInformation  @303
```